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Nonlinear device characterization and second harmonic impedance tuning to achieve peak performance for a SiC power MESFET device at 2GHz

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Nonlinear device characterization and second harmonic impedance tuning to achieve peak performance for a SiC power MESFET device at 2GHz

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ABSTRACT

This thesis presents a way to make nonlinear device measurements for a power MESFET device using the load pull system. The device was characterized at the fundamental and second harmonic frequencies during large signal operation. The data thus collected was used in designing the input and output impedance matching networks that would optimize the performance of the device. A power MESFET device like the one used to conduct this experiment is mainly used in designing power amplifiers for communication systems including the transmitters used in satellites. Therefore efficiency of the part is of the utmost importance. By characterizing the device and utilizing matching impedance networks on the input and the output of the device, the efficiency of the device can be greatly improved. The characterization of the device, the construction of the matching networks, simulation and test results for the output power are all presented in this thesis.

CHAPTER 1. OVERVIEW

Load pull is an automated measurement technique used to make measurements on a device under test (DUT) while under operating conditions. This is a very important measurement technique utilized for large signal, non linear devices [1]. Device characterization by load pull is a means of identifying the conditions, by measurement, under which the device has the optimum performance. By characterizing the device, optimal circuits can be designed to operate under conditions that result in maximum performance. Characterizing a non linear device is particularly difficult because the absence of linearity means that the relationships between the device terminals are no longer simple [2]. In the case of linear devices, characterization is not a problem because the small signal S-parameters can usually be used to predict the performance at various loads. Several methods have been proposed for characterizing non-linear devices. The load pull is one such technique that allows the user to characterize a large signal, non-linear device while under operation [1].

1.1 Introduction to Load Pull

Load pull consists of changing the load impedance seen by the DUT and measuring the device operation simultaneously. This technique is called load pull because the load impedance is varied or "pulled" using a load tuner. Similarly, the source impedance can also be varied using a source tuner when making measurements of the device performance. This is called source pull [1]. Load pull and source pull are often used to characterize microwave and RF power devices. The device itself is characterized with respect to the input source impedance and output load impedance using the corresponding automated tuner since impedance is a parameter that relates to voltage, current and power. Devices can be characterized with respect to impedance for noise figure, gain, output power, efficiency, linearity, etc [3].

1.2 Problem Statement

SiC rf power devices capable of operating at temperatures in the 200˚C range have recently become available. The main objective of this research project was to characterize

these new devices for best performance. The DUT that was used is the CREE CRF24010F. This is a 10 W, unmatched silicon carbide (SiC) RF power Metal Semiconductor Field-Effect Transistor (MESFET). This device has various applications including a wide range of uses in the field of communications. It can also be used in the design of class A, A/B power amplifiers, CDMA, TDMA, EDGE, broadband amplifiers, etc [4]. Looking at the areas of application for this device, it is clear that the output power and efficiency of the device are critical performance parameters of this device. Therefore characterizing the device for maximum output power will significantly improve device performance. The measurements for this device were made at a fundamental frequency of 2GHz using harmonic load pull at 4GHz.

1.3 Approach

The approach taken to improve the device circuit performance was to tune the input and output impedance for the best match. This improves the device performance. Since the particular SiC MESFET device that is used in this project is a square law device, the device generates second harmonics. Therefore, in addition to characterizing the DUT at the fundamental frequency with respect to impedance, the DUT can also be characterized at the harmonic frequencies with respect to impedance as well. The device's circuit performance can further be optimized by characterizing the device at the second and third harmonic frequencies with respect to impedance. In recent years, harmonic load and source pull has been gaining in popularity [5]. Harmonic load pull can be important in optimizing the efficiency and linearity of the device where as harmonic source pull can be important in optimizing the device performance by controlling the amount of harmonic generation. Harmonic source pull is just as important as harmonic load pull, especially in cases where performance is critical [5].

1.4 Overview of the device characterization procedure

The device used in the study was first measured for output power at the fundamental frequency of 2GHz using the load pull technique. By setting the load and source tuner at the optimum load and source impedances, the maximum output power for the device along with the efficiency for the device was measured and recorded. The setup was then changed to

include harmonic source pull as well. The additional second harmonic tuner was adjusted for an optimum impedance along with the load and source tuners. After an optimum harmonic termination was achieved, the input matching network and the output matching network corresponding to the established optimum tuner positions was measured. These measurements are then used to construct input and output matching networks for the device using standard rf and microwave circuit synthesis techniques. The same device is then connected to the optimum input and output matching network that was constructed in order to verify that the device produces the same output power as measured with load and source tuners. The setup, measurement techniques, results and an analysis of the results will be presented in later sections of this thesis.

1.5 Literature Review

During the process of searching for publications in this area, something that was noticeable was the fact that research using load and source pull measurement techniques is limited. Even though these types of measurements are gaining more popularity in recent years, there is still a lot of progress that can be made. From my experience working with the load pull setup, this is an underutilized technique. As the need for RF circuits increases in the future, the research using the load pull measurement technique should also increase.

One of the major uses of load pull measurement techniques is in designing power amplifiers. When designing a power amplifier used in communication circuits, efficiency is a very important parameter to consider. High efficiency requires large signal operation of the device. The advantage of using a load pull technique is that the device can be measured under actual large signal operating conditions. Load pull measurements are often used in making measurements to determine the matching impedances that are needed for optimum power amplifier design. These matching networks are then created and connected to the input and output of the DUT to extract the best performance of the DUT. Usually the matching impedance is measured and synthesized at the fundamental frequency, but matching impedances at the harmonic frequencies often improves the performance of the device significantly [6]. One of the papers that was reviewed, [6], uses a BJT as the DUT to make

output power and efficiency measurements before and after load pull, utilizing matching networks at the fundamental and second harmonic frequencies.

CHAPTER 2. SETUP

load and source pull measurement techniques require a very elaborate setup. This includes automated tuners for the load and source impedance, signal generators, power supplies, a high isolation switch, power meter, oscilloscope, spectrum analyzer, etc. Two different types of setups were used when characterizing the DUT used in this study. The first one was a setup used to make output power measurements after tuning the source and load tuners for optimum impedances over a range of frequencies including the fundamental frequency of 2GHz. The other setup was the second harmonic source pull setup that allows the load, source and the second harmonic tuners to be set to optimum impedances. The two setups are similar, but with significant differences between them. In this chapter, the techniques that were used to make these measurements as well as the different components of the load pull setup for the two different configurations are described. An overall picture of the setup is shown in Appendix 1.

2.1 Measurement Technique

The load pull system that was used for the power and harmonic measurements utilized pulsed bias and pulsed RF signals. The pulsed bias and pulsed RF signals were used in order to minimize the risk of DUT burn out and to limit the temperature rise of the MESFET die. The pulsed signals are turned on for 10μs and turned off for 1ms. The measurements were made when the pulsed bias and RF signals were "on." On the load pull system, the pulsed bias and pulsed RF signals were achieved using a custom built pulse generator and high isolation switch as shown in Fig 1 and Fig 2 [7].

2.2 Instrument Setup

Load pull and source pull measurements were made using an automated tuner setup to do the measurements. The automated tuner system (ATS) had been purchased from Maury Microwave Systems. This system consists of a tuner controller, two tuners and software to control these instruments. The software that is provided with this initial setup is called SNPW. The different setups require different configurations, but the instruments that were used were all the same. A general purpose interface bus (GPIB) is used to communicate between the instruments and the SNPW software. Some of the instruments and their GPIB

addresses that were used for making these automated measurements are as shown in Table 1.

Table 1: Instruments used in the load and source pull measurements

Instrument Type	Model Number	GPIB Address
Tuner Controller	MT986B02	11
Network Analyzer	W37300	6
Output Power Meter	HP4418A	13
RF Power Source	HP8648C	19
Spectrum Analyzer	HP8560A	20
GPIB Board	PCI-GPIB	0

In addition to these instruments, a few power supplies were used to set the bias for the device as well. These instruments were used in both the initial load pull measurements as well as the harmonic source pull measurements.

2.3 Biasing the Device

The SiC MESFET that was characterized is a depletion mode part. In depletion mode parts, the gate bias that is applied is negative. The negative voltage at the gate will repel electrons (because of their negative charge) away from the gate. This creates a depletion region around the gate region because electrons are the majority current carriers in n-type silicon. By depleting the gate region, the size of the channel is reduced and the current flow is also reduced. Increasing the negative gate voltage decreases the channel size which in turn decreases drain current flow. Decreasing the negative gate voltage increases the channel size which in turn increases drain current flow. The bias conditions used for the DUT used in this study are shown in Fig 1.
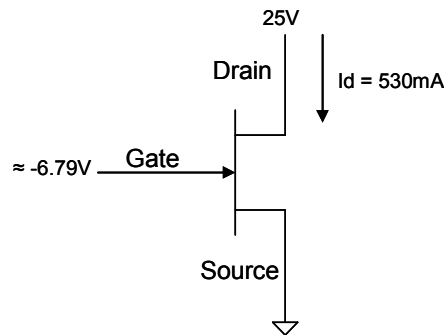
Figure 1: DUT - Depletion mode SiC MESFET device biasing

During the measurements the drain to source voltage was biased at 25V and the drain current was biased to be 530 mA. The gate voltage was adjustable such that it varied over several milli-volts in order to satisfy the drain current setting of 530 mA. The average gate voltage for the DUT used was around -8V. A measured I-V curve for the device is shown in Fig 2.

V-I curves for CRF24010F
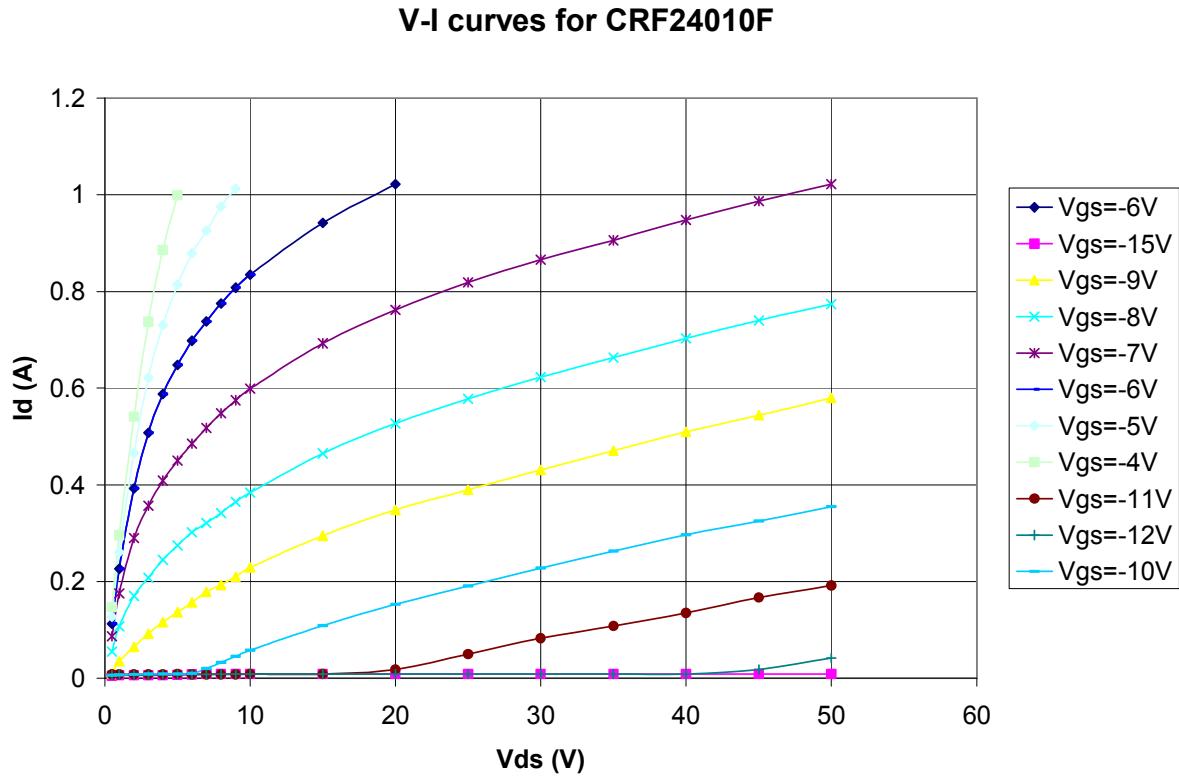
Figure 2: Measured I-V curves for the DUT (pulse operation, 10us, 1% duty cycle)

2.4 Initial load pull Measurement Setup

For the initial load pull measurements, the system was setup to measure output power and efficiency of the MESFET. The setup used to do these measurements is shown in Fig 3.

```
┌──────────────┐        ┌──────────────┐
│    Signal    │        │              │
│  Generator   │        │ Power Supply │
└──────┬───────┘        └──────┬───────┘
       │                       │
       ▼                       ▼
┌──────────────────────────────────────┐        ┌──────────────────────────┐
│ RFin                            DC+   │        │                          │
│                                       │        │      Custom Built        │
│         High Isolation Switch         │        │     Pulse Generator      │
│                                       │        │                          │
│ RFOUT   TTL      DC-    RFOUT2        │        │ RF                  Bias │
└──────────────────────────────────────┘        └──────────────────────────┘
```

| 1W Amp | → | Coupler | → | Circulator | → | 2W Amp | → | Circulator | → | Coupler | → | Input Bias Tee |

| Source Tuner | → | Coupler | → | **DUT** | → | Coupler | → | Load Tuner | → | Output Bias Tee | → | Output Power Meter |
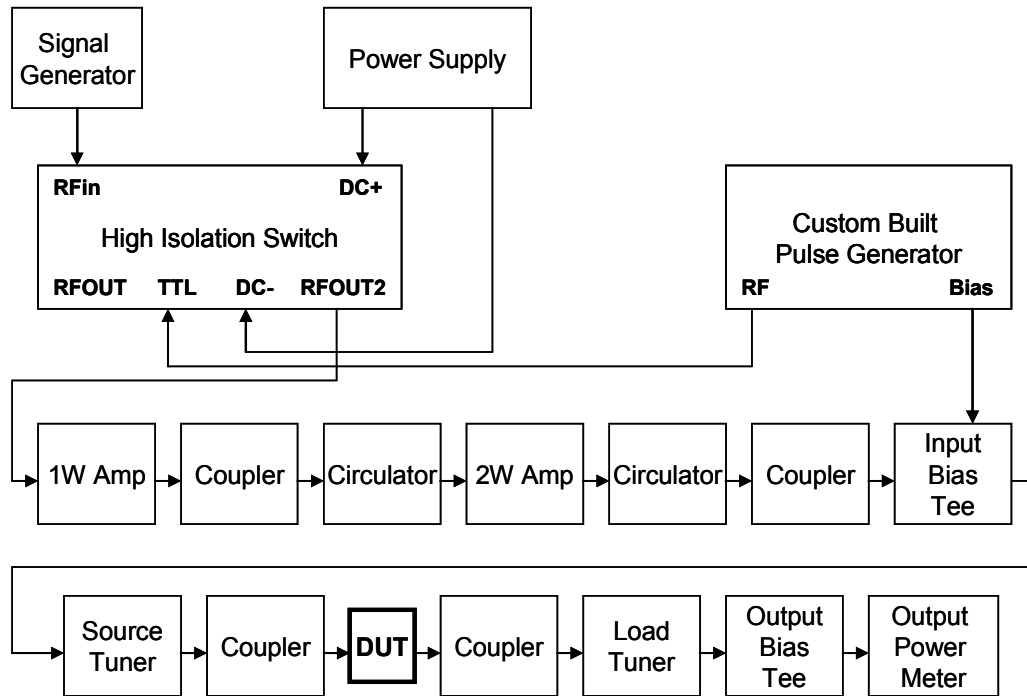
Figure 3: Load pull setup for measuring output power

The device was placed in a 5 ohm fixture customized for this particular device. On the input gate side, the fixture was connected to a male-to male connector followed by a coupler which was connected to a male-to-male connector before it was connected to the source tuner. On the output drain side, the fixture was connected to a male-to-male connector, then to a coupler that is in turn connected to a load tuner. The source tuner and load tuner were connected to a tuner controller. The tuner controller itself was connected to the computer through GPIB cables. The SNPW software was used to control the tuner position of the load and source tuners. The input bias tee used to apply gate bias to the DUT was connected to the input of the source tuner and the output bias tee used to apply the drain bias on the device was connected to the load tuner output. The high isolation switch and the custom built pulse generator seen in Fig 3 were used to generate the pulsed signal for the bias and RF signals as described in Section 2.1. The 1W and 2W amplifiers on the gate of the device were used to increase the input power available. Sufficient power available at the input of the device was necessary to produce high output power, which was the major objective for the device characterization. On the output drain side, the output power is

measured using a power sensor that was in turn connected to an output power meter where the power was displayed [7]. The power that is displayed on the output power meter is not the true output power because of losses in the system; these losses need to be accounted for as well. Using a one percent duty factor results in an effective 20 dBm of power loss when using pulsed bias and rf signals and there is another 20 dBm attenuator used in the output system setup. These losses were accounted for by adding 40 dBm to whatever the power meter reads. This allows the true power out at the drain terminal of the DUT to be computed after the de-embedding is complete. The 40 dBm power loss was accounted for by adding this to the output power meter display if the load pull measurements were done manually. If the automated SNPW software was used, then losses were automatically accounted for in the output that the software displayed. This is because the system is configured and each and every device that is added to the system (any device that is not the DUT but is still part of the test system setup) is accounted for by initially characterizing the device and integrating the S-parameter file for the device in the workbench of the SNPW software when initializing the system.
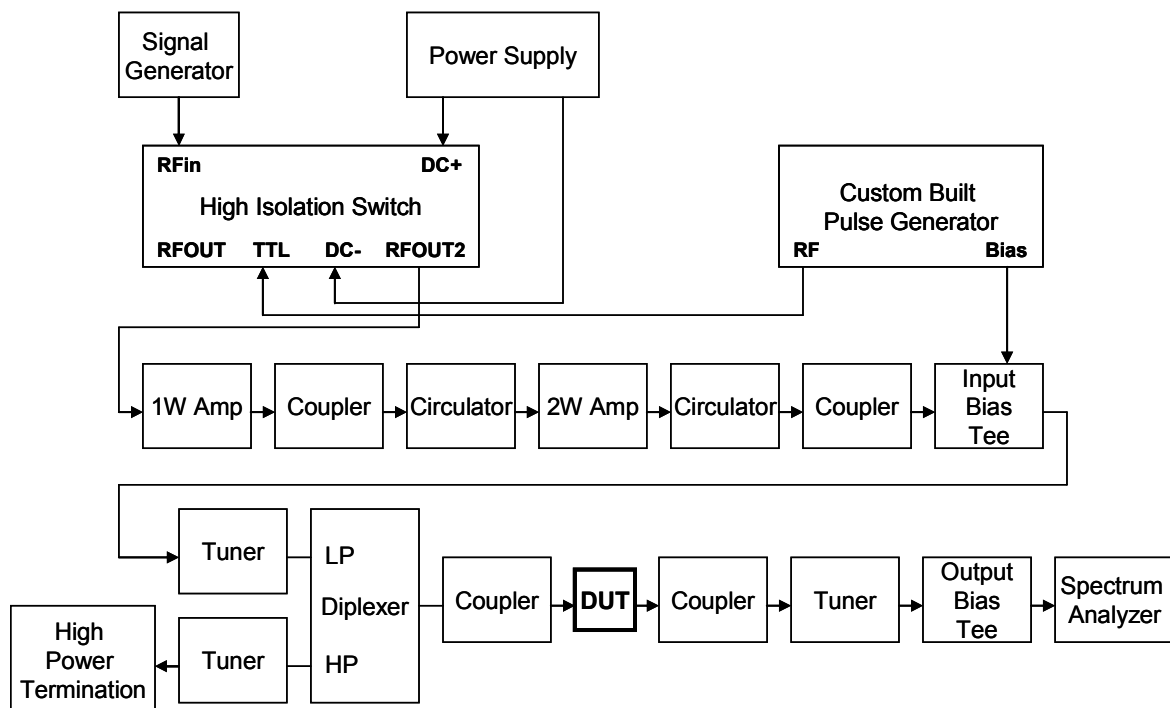
Figure 4: Second harmonic source pull measurement setup

2.5 Second harmonic source pull measurement setup

The setup for the second harmonic source pull measurements was very similar to the initial load and source pull measurement setup from Fig 3. Fig 4 shows the slightly modified setup used to make second harmonic source pull measurements.

There is very little difference between the initial setup used to measure output power, gain and efficiency and the setup used to make second harmonic source pull measurements. The major difference is in the addition of a diplexer and a second harmonic tuner. The diplexer was used to separate the diplexer signal path at the fundamental frequency of 2 GHz and the second harmonic frequency of 4 GHz. The diplexer design is discussed in section 3.2.1 in more detail. The second harmonic tuner was connected to the 4GHz port of the diplexer and the other end of the tuner was terminated with a high power 50 Ohm termination [5]. The output power meter from the initial setup was replaced with a spectrum analyzer so than the power at 2 GHz and 4 GHz can be measured separately.

CHAPTER 3. DESIGN AND MEASUREMENTS

This section explains in detail the procedure and techniques used in making the load and source pull measurements. It also describes the design of the diplexer and matching networks that were utilized in the second harmonic source pull measurements.

3.1 Fundamental frequency load pull measurement

Each tuner position corresponds to certain impedance. The tuner positions set the input and output impedances of the DUT. By changing the tuner positions either manually or automatically using the SNPW software, the input or output impedances was changed and set at the optimal position that provided the maximum output power. The load pull was run with the source tuner set at the optimum source impedance position. The results obtained from these measurements correspond to the output power at various tuner positions that in turn corresponds to various load impedances for a set frequency and bias condition. By running a load pull using constant optimum source impedance, the varying output power results corresponding to various load impedances were displayed as contours on a Smith Chart®. The point that corresponds to the maximum output power was considered the optimum load impedance. Therefore, the optimum source and load impedance for the device at a certain frequency and bias condition was obtained automatically minimizing tedious, long and tiresome manual data collection [7].

3.1.1 Measured Results

Initially, the second harmonic content of the signal was not taken into consideration. The CREE CRF24010F device's output power measurements were obtained at a range of fundamental frequencies to look at the device operation and the device capabilities. The range of frequencies chosen was from 1.8 GHz to 3.0 GHz. All measurements were made with the device bias set at Vds = 25V, Ids = 530mA and Vgs ≈ -8V. At each of the frequencies chosen, the device was biased at the set conditions, and the optimum source impedance was found. This was set by manually changing the source tuner until the maximum optimum power was achieved. The impedance corresponding to the tuner position that achieved maximum output power is recorded as the optimum source impedance. With

the source tuner fixed at this optimum impedance position, the load tuner was varied using the automated SNPW program and the results thus obtained for output power, efficiency and gain were plotted on a Smith Chart to show the load circles. The optimum load impedance for the device was also found by looking at the results and finding the load impedance that provided the maximum output power and efficiency. The optimum source and load impedances that were thus obtained are tabulated and shown in Table 2. The optimum source impedance and load impedance circles are also shown in Fig 5 [8]. The load pull circles that were obtained from the automated SNPW program for a fundamental frequency of 2.0GHz are included in Appendix 2.

Table 2: Optimum load and source impedances of the DUT at Vdd=25V and Ids=530mA

Frequency (GHz)	Source Impedance (Ω)		Load Impedance (Ω)	
	Real	Imaginary	Real	Imaginary
1.8	3.69	2.92	3.1	9.63
1.9	4.69	3.6	2.63	8.57
2	2.33	2.78	3.79	6.37
2.1	2.1	1.32	3.3	6.36
2.2	2	1.86	3.15	3.02
2.3	2.62	-0.19	2.07	3.58
2.4	2.94	0.48	1.77	1.93
2.5	2.71	-0.56	1.42	0.6
2.6	3.82	-2.25	1.19	1.46
2.7	5.2	-2.35	2.98	-0.02
2.8	4.04	-2.33	4.9	0.28
2.9	3.92	-3.36	3.74	-2.28
3	4.83	-3.56	4.63	-5.49

m1
freq=1.800GHz
S(1,1)=0.780 / 51.229
impedance = Z0 * (0.620 + j1.926)

m2
freq=2.300GHz
S(1,1)=0.584 / 102.442
impedance = Z0 * (0.414 + j0.716)

m3
freq=2.600GHz
S(1,1)=0.642 / 145.762
impedance = Z0 * (0.238 + j0.292)

m4
freq=2.800GHz
S(1,1)=0.030 / 108.034
impedance = Z0 * (0.980 + j0.056)

m5
freq=3.000GHz
S(1,1)=0.496 / -64.168
impedance = Z0 * (0.926 - j1.098)

freq (1.800GHz to 3.000GHz)
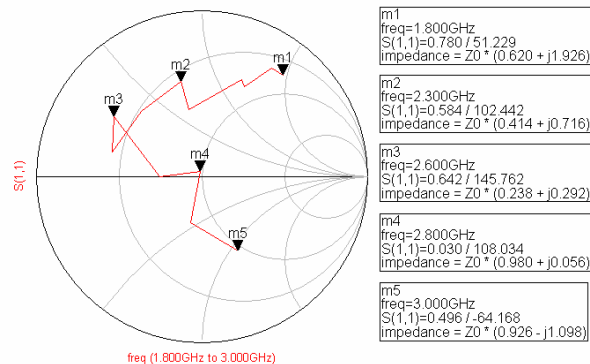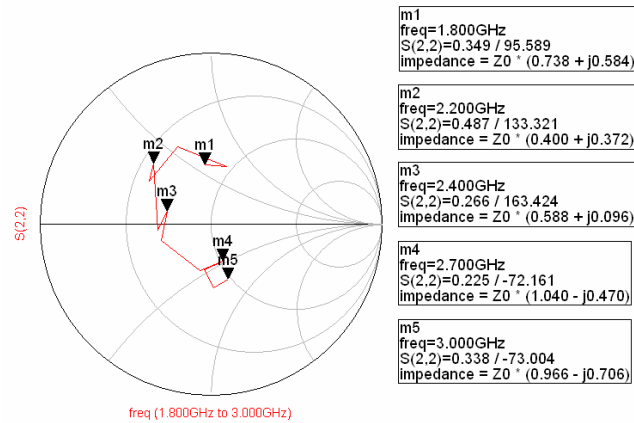
Figure 5: Optimum load impedances for DUT (left chart) , Optimum source impedances for DUT (right chart)

When making load-pull measurements, a new problem was noticed. When certain impedances on the load circle were chosen, the drain current changed from the original setting, thus making the data recorded useless. Since the bias was set to Id = 530mA, any dramatic change in the bias would disrupt a proper load pull measurement as load circles are supposed to have the same bias along the contours. Since the input drive of the device is changed within a pre-set range during load pull, the bias change problem was investigated further by exploring the relationship between input drive and the drain current. The following sections will include measured data as well as simulated data of the relationship between input drive and drain current. It also includes a theoretical analysis and a description of a possible reason for this condition.

3.1.1.1 Relationship between input drive and drain current – Measured Data

Since the drain current of the MESFET was observed to change when the input drive was changed, the relationship between these two variables was further investigated. The drain current was measured as a function of input power for the device at 2.0 GHz with the load and source tuners set at the optimum load and source impedance positions. Multiple measurements were made to verify the trend. Measurements were made by first turning off the input power and adjusting the Vgs value to obtain an Ids current of 150mA, 200mA and 300mA at dc and then gradually changing the input power and recording the corresponding Ids values while Vgs was held constant. The data thus obtained is shown in Fig 6.

Pin vs. Ids
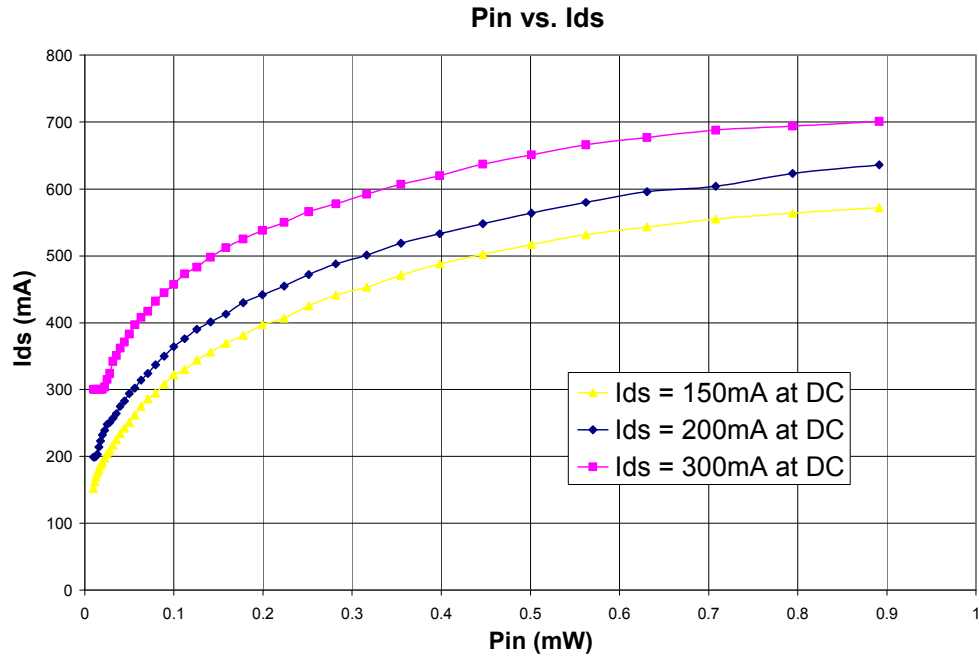
Figure 6: Measured input drive vs. drain current relationship at 2.0GHz

3.1.1.2 Relationship between input drive and drain current – Simulated Data

A model of the SiC MESFET device was used to obtain simulated results. Simulation was done to verify that the measured data matched the simulation results. The result from the simulation is shown in Fig 7. This curve matches the trend of the measured results shown in Fig 6.

Pin vs. Ids
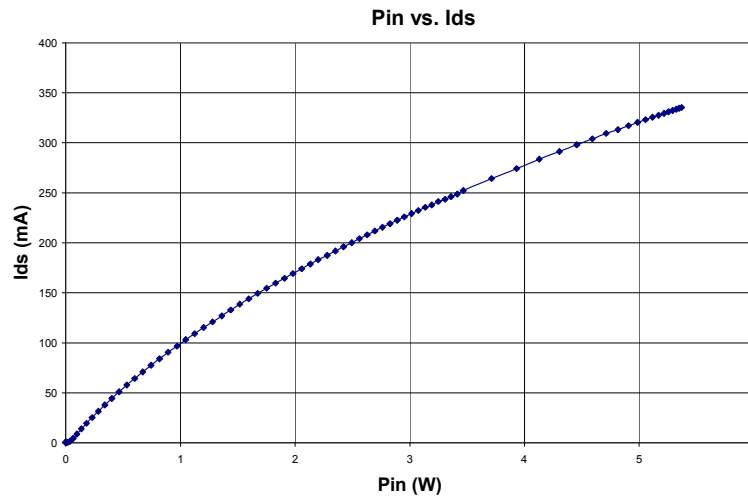
Figure 7: Simulated input drive vs. drain current relationship at 2.0GHz

Fig 8, depicts the I-V curves that were simulated using a device model and the I-V curves that were measured under pulse operation for the MESFET device. With the exception of a slight difference in the threshold voltage, the measured and simulated values are a close match. The difference seen at higher voltages may be due to the device's temperature rise difference between CW and pulse operation.
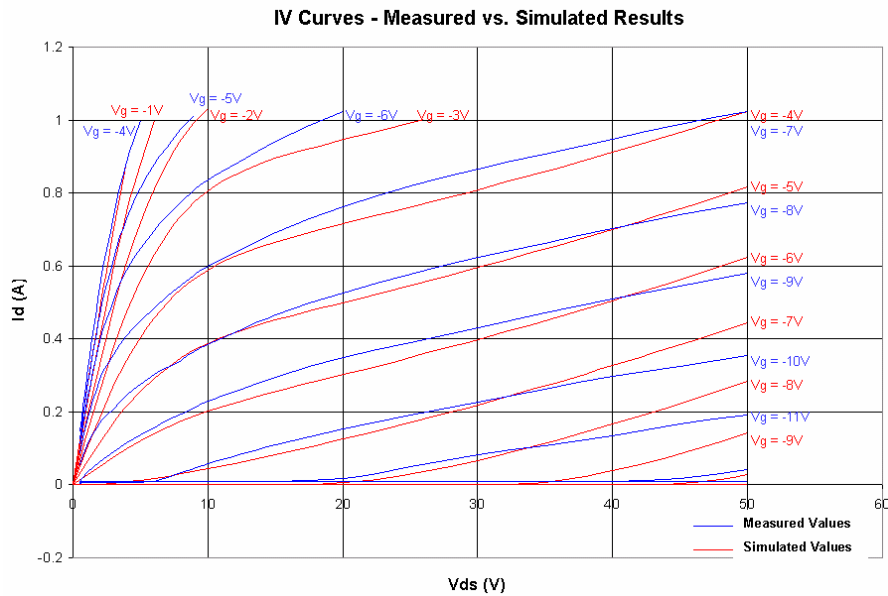
Figure 8: Measured and simulated I-V curves for the DUT

3.1.1.3 Relationship between input drive and drain current – Theoretical Analysis

A theoretical analysis was also done to confirm that trends seen in the measured and simulated data for the input power vs. drain current relationship have a theoretical basis. Using the approximate MESFET equations [9],

$$I_{DS} = K(V_{GS} + V_T)^2 \tag{1}$$

where,

$$K = \frac{I_p}{V_p^2} \quad \text{and,} \tag{2}$$

$$V_T = V_p + V_{B1} \tag{3}$$

In these equations,

I_p is the pinch-off current,

V_p is the pinch-off voltage, and

V_{B1} is the built-in gate voltage.

Substituting and simplifying these equations results in,

$$I_{DS} = K\left(V_{GS} + (V_p + V_{B1})\right)^2 \tag{4}$$

In the high input power situation, V_{GS} can be written as,

$$V_{GS} = A\cos(\omega t) + V_{gso} \tag{5}$$

Substituting (5) into (4) gives,

$$I_{DS} = K\left((A\cos(\omega t) + V_{gso}) + (V_p + V_{B1})\right)^2 \tag{6}$$

$$I_{DS} = K\left((A\cos(\omega t)) + (V_{gso} + V_p + V_{B1})\right)^2 \tag{7}$$

Assume that

$$C = V_{gso} + V_p + V_{B1} \tag{8}$$

then (7) can be re-written as,

$$I_{DS} = K\left((A\cos(\omega t)) + C\right)^2 \tag{9}$$

Expanding (9) results in,

$$I_{DS} = K\left[(A^2\cos^2(\omega t)) + 2(A\cos(\omega t))(C) + C^2\right] \tag{10}$$

$$I_{DS} = K\left[\left(\frac{A^2}{2} + \frac{A^2\cos(2\omega t)}{2}\right) + 2AC(\cos(\omega t)) + C^2\right] \tag{11}$$

Where C is given by (8) and C^2 is given by (12) below:

$$C^2 = V_{gso}^{\;2} + V_p^{\;2} + V_{B1}^{\;2} + 2V_{gso}V_p + 2V_{gso}V_{B1} + 2V_pV_{B1} \tag{12}$$

Substituting (8) and (12) back into (11) results in

$$I_{DS} = K\left[\frac{A^2}{2} + \frac{A^2\cos(2\omega t)}{2} + \left(2AV_{gso} + 2AV_p + 2AV_{B1}\right)\cos(\omega t)\right.$$

$$\left. + V_{gso}^{\;2} + V_p^{\;2} + V_{B1}^{\;2} + 2V_{gso}V_p + 2V_{gso}V_{B1} + 2V_pV_{B1}\right] \tag{13}$$

$$I_{DS-dc} = K\left[\frac{A^2}{2} + V_{gso}^{\;2} + V_p^{\;2} + V_{B1}^{\;2} + 2V_{gso}V_p + 2V_{gso}V_{B1} + 2V_pV_{B1}\right] \tag{14}$$

When $\dfrac{A^2}{2} \gg C$, $\qquad I_{DS-dc} = K\dfrac{A^2}{2} \tag{15}$

Looking at (13), at dc, the amplitude of the input sinusoidal signal has a significant effect on the drain current. This dc offset caused by the input signal is one reason for the changes in the drain current and therefore causes changes in the drain bias current during load pull measurements. The relationship portrayed by (15) does not perfectly match the simulated and measured results.

The initial theory was that the Ids equation used to do this analysis is a simple representation of the actual model. In reality there are other variables that may influence the relationship between drain current and the input drive.

A more complex and accurate model will depict this relationship better. Further analysis was done and (1) was replaced with a drain current equation that included the early voltage effect and the derivation was repeated to see the changes in this relationship. Fig 9 shows a general Ids vs. Vds relationship for a MESFET. In this figure, the early voltage is depicted using the variable V_A. This figure is mainly used to show the variables used when deriving the Ids equation [10].
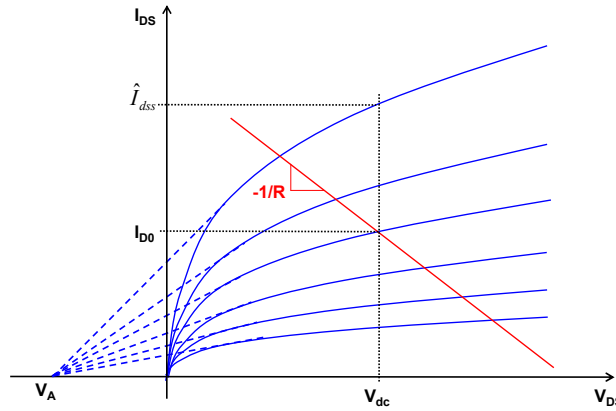
Figure 9: I-V curves for the DUT displaying variables used in theoretical analysis

Using this figure and after careful derivation, the Ids equation that was arrived at is shown in (16)

$$I_{DS} = \left(\frac{\dfrac{\hat{I}_{dss}}{V_{DC}-V_A} \dfrac{(V_g-V_T)^2}{V_T^2} \dfrac{V_A}{I_{do}} + 1 - \dfrac{V_{DC}}{I_{do}R}}{-\dfrac{\hat{I}_{dss}}{V_{DC}-V_A} \dfrac{(V_g-V_T)^2}{V_T^2} R + 1} \right) + \frac{V_{DC}}{R} + I_{do} \tag{16}$$

The input signal can be estimated to be similar to (17) below.

$$V_g = V_{go} + A \cos(\omega t) \tag{17}$$

$$V_g - V_T = V_{go} - V_T + A \cos(\omega t) \tag{18}$$

$$(V_g - V_T)^2 = (V_{go} - V_T)^2 + 2A \cos(\omega t)(V_{go} - V_T) + A^2 \cos^2(\omega t) \tag{19}$$

$$= (V_{go} - V_T)^2 + 2A \cos(\omega t)(V_{go} - V_T) + \frac{A^2}{2} + \frac{A^2 \cos(2\omega t)}{2} \tag{20}$$

Substituting (20) into (16) and looking at the dc value, (21) can be obtained.

$$I_{DS-dc} = \left(\frac{W + XA^2}{Y + ZA^2} \right) + K \tag{21}$$

where,

$$W = \frac{\hat{I}_{dss} V_A (V_{go} - V_T)^2}{(V_{DC} - V_A) I_{do} V_T^2} + - \frac{V_{DC}}{I_{do} R} + 1 \tag{22}$$

$$X = \frac{\hat{I}_{dss} V_A}{2(V_{DC} - V_A) I_{do} V_T^2} \tag{23}$$

$$Y = - \frac{\hat{I}_{dss} R (V_{go} - V_T)^2}{(V_{DC} - V_A) V_T^2} + 1 \tag{24}$$

$$Z = - \frac{\hat{I}_{dss} R}{2(V_{DC} - V_A) V_T^2} \tag{25}$$

$$K = \frac{V_{DC}}{R} + I_{do} \tag{26}$$

The relationship shown in (21) still does not perfectly match the trends from the simulation and measurements. However, when performing this analysis, it was discovered that the assumptions made about the MESFET in Fig 9 did not match the actual results. In Fig 9, it is assumed that the early voltage, V_A, is constant voltage that does not have any relationship to Vgs. However, when examining the simulation and measured results, this is not the case. The early voltage changed as a function of Vgs. The analysis performed using (16)-(26) needs to take this relationship into account as well. This will have a definite impact on the final Ids vs A relationship shown in (21). Once the relationship between the two variables is determined, a more accurate theoretical analysis of drain current vs. input drive could be obtained.
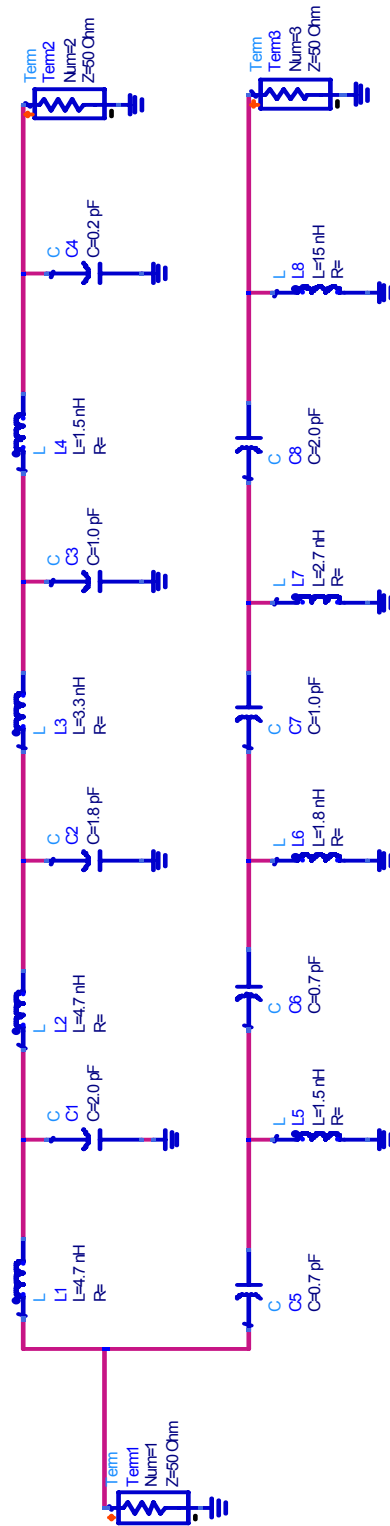
Figure 10: 8-pole diplexer schematic

3.2 Second harmonic source pull measurement

The main goal of this research project was to increase the device circuit performance. This is mainly done through impedance tuning at the fundamental frequency and constructing a matching network using the optimum impedances. Some investigators have discovered that second harmonic tuning also has a significant impact on the performance of the device [5]. Therefore, a process similar to the fundamental frequency impedance tuning was adapted for the second harmonic tuning as well. The diplexer in the setup separates the fundamental and second harmonic frequencies. The fundamental frequency port of the diplexer is connected to the fundamental impedance tuner whereas the second harmonic frequency port of the diplexer is connected to the second harmonic impedance tuner. Before tuning the second harmonic tuners, the fundamental source tuner and the load tuner are set at optimum impedance positions derived from the initial sets of measurements. This value slightly changes due to the addition of a diplexer in the setup. After the fundamental source tuner and the load tuner positions were tuned for the maximum output power values, the second harmonic tuner was also tuned to the position that provides the maximum output power. The criteria might be minimum harmonic generation or maximum efficiency or both. Once all tuners are set to the optimum impedance positions, the device should be at its best performance [5].

When the optimum impedances set by the tuners were known, the input and the output impedance seen by the DUT was derived. It is necessary to characterize each and every device between the input bias and the DUT's gate terminal on the input side and characterize all devices between the DUT's drain terminal and the output bias on the output side. The resulting device impedances are used to embed the impedance seen by the DUT on the input and the output side. This was done using Agilent's Advanced Design Software (ADS) software. The actual setup of the devices and the embedded impedance results are included in Appendix 3, 4 and 5.

In the case of the test fixture, the fixture was characterized as a whole. Since the DUT was placed in the middle of the fixture, the S-parameter files for the individual halves were needed in order to perform impedance embedding. Assuming that the individual halves of the

fixture were mirror images of each other, the S-parameters for each half of the fixture was calculated. The calculation procedure is included in Appendix 6.

3.2.1 Diplexer Design

When making second harmonic source pull measurements, a diplexer was used on the gate side in order to separate the fundamental frequency from the second harmonic frequency. "A frequency diplexer is a multiport network that takes input composed of several frequencies at one port and produces outputs at other ports with those outputs containing frequencies only in selected frequency bands" [11]. An 8-pole frequency diplexer was designed to enable second harmonic measurements and tuning. The circuit was simulated using ADS. RETMA values were used for the lumped component values. The corresponding circuit is shown in Fig 10. This circuit was later modified to include pads and component parasitcs. The resultant circuit was simulated and the simulated results thus obtained are shown in Fig 11.
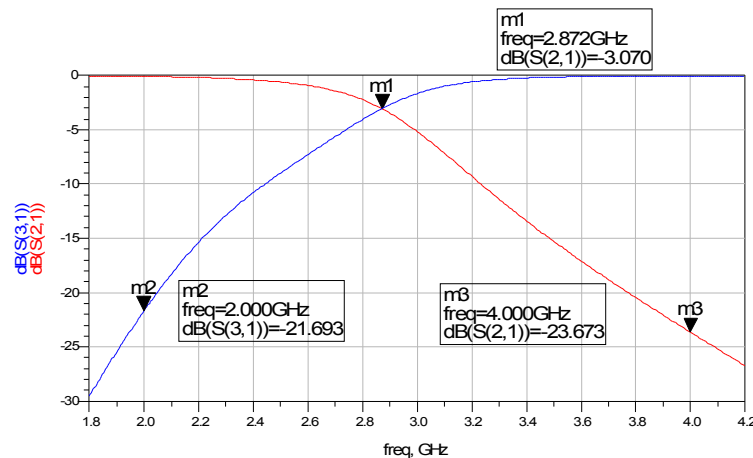
Figure 11: Simulation results for diplexer

The diplexer circuit that was designed was then constructed and tested. Fig 12 shows the results that were measured from the diplexer circuit using the network analyzer.
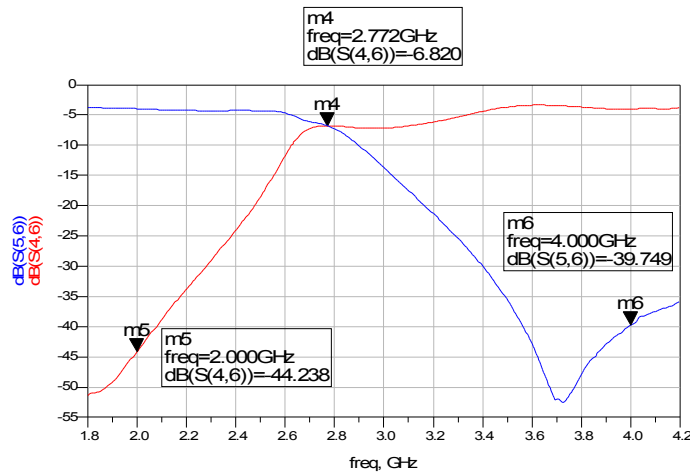
Figure 12: Measured results for diplexer

The measured data from the constructed circuit closely matched the simulation results shown in Fig 11.

3.2.2. Harmonic source pull measurements

When making second harmonic load or source pull measurements, there are two steps. Initially, the source pull was done using the automated tuners by setting the load and fundamental frequency tuner at the optimum impedances and adjusting the second harmonic tuner. The measured results for second harmonic power were recorded corresponding to the second harmonic tuner position. The automated tuners have three different variables that can be changed. These are listed as P1, P2 and L. Changing each of these variables results in the tuner position being moved up or down and back or forth. P1 represents the position with, respect to the line, of a large capacitance slug on the slide screw tuner, P2 represents the position with respect to the line of a smaller capacitive slug and L represents the lateral position of the slug carriage on the line. When measuring the second harmonic power of the device, the tuner position P1 was set at 5000 (completely withdrawn) and P2 was changed to the following values: 20, 250, 500, 1000, 1500, 2000, 2500. For each of these P1, P2 combinations, L was changed from 0 to 21000 and the output second harmonic power was recorded at finite intervals of this L position. The impedances measured at the tuner and the embedded impedances measurements at the DUT corresponding varying P2 and L values are

plotted on Smith Charts and are included in Appendix 7. The plot of L position vs. output second harmonic power is shown in Fig 13 for the condition that P1 = 5000 and P2 = 20.

Measured Changes in Second Harmonic Power as a Function of Tuner 'L' Position
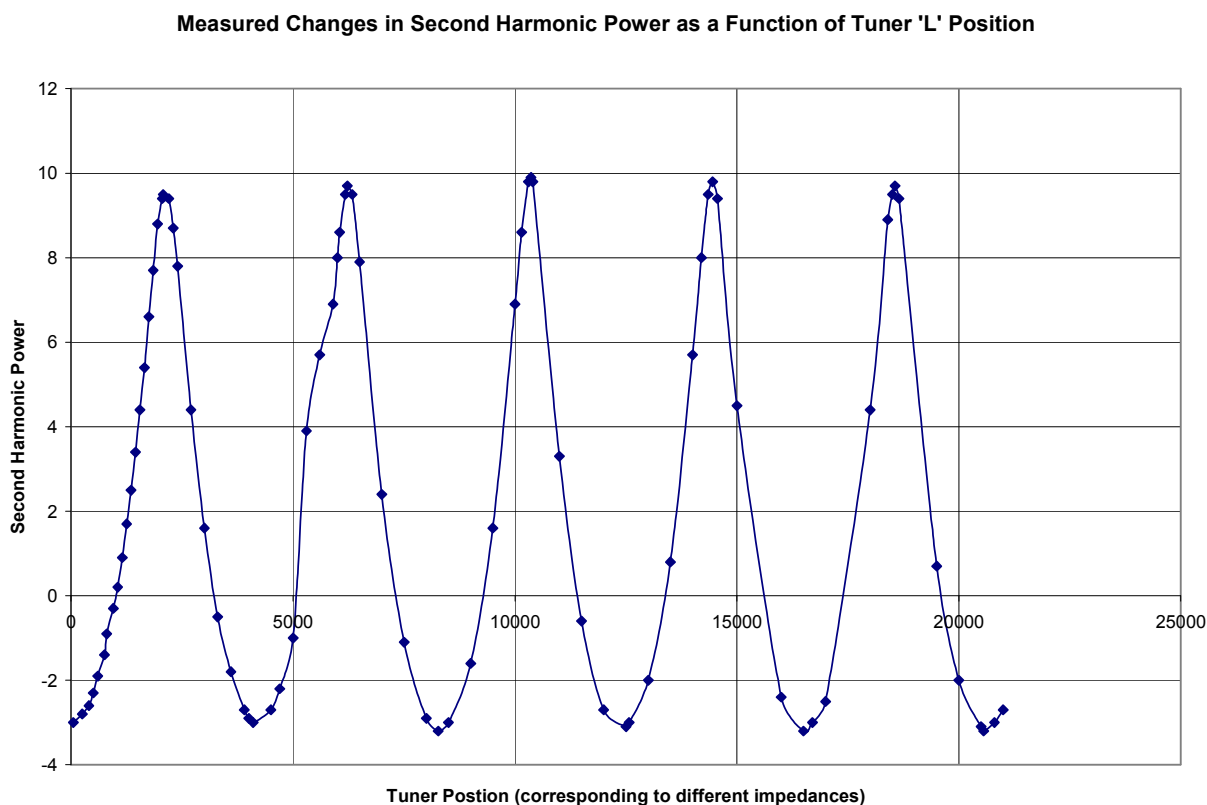
Figure 13: Second harmonic output power vs. tuner "L" position

Looking at the plot, the relative second harmonic power varies over a range of 12.9 dB (from 9.7 to -3.2 dBm) when measured as a function of second harmonic input impedance. The second harmonic tuner was characterized using a network analyzer and the impedance corresponding to each of the tuner positions was measured and recorded. Thus, the second harmonic power is known with respect to the impedance at the tuner.

Since the DUT was being characterized, the input and output impedances at the DUT had to be calculated. The impedance found at the tuners was embedded all the way up to the DUT. This was done using ADS as explained in the previous section. The embedded input and output impedances are then used to design the input and output matching networks at the fundamental and second harmonic frequencies. The matching network design technique is explained in the following section. Appendix 8 shows the table with tuner positions,

corresponding impedances at the tuners, the embedded impedances at the DUT and the second harmonic output power that was measured. This constitutes the data that was collected using the source pull measurement technique.

3.2.3. Matching Network Design

As explained in the earlier sections, the tuners were set to their optimum impedance positions and the corresponding input and output impedances were noted and embedded all the way to the device input and output termination. The matching network is designed corresponding to the embedded input and output impedances. To design the matching network, the Q^2+1 method was used. Fig 14 shows a simple model that can be used for designing the input and output matching networks [11].
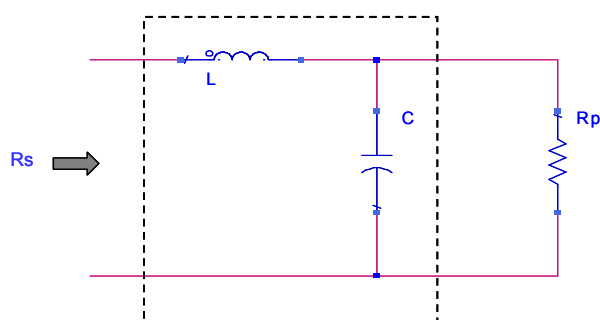
Figure 14: Simple matching network model used for input impedance matching

From the embedded impedance measurements, the input and output impedances were at a 2 GHz fundamental frequency as follows:

- Fundamental frequency optimal input impedance: 19.847 + j 3.636 Ohms
- Second harmonic optimal input impedance: 7.157 + j 53.478 Ohms
- Output optimal impedance: 108.537 – j 10.417 Ohms

For the purposes of this project, the input and output impedances are all matched to 50 + j0 Ohms. In the case of the matching network for the fundamental frequency optimal input impedance, the design steps are as follows:

The first step is to get rid of the imaginary part of the impedance. The input impedance is of the form:

R + jX, where R is the resistance and the X is the reactance. In this case, R = 19.847 Ohms, X = 3.636 Ohms. Reactance can be converted to lumped components as follows:

$$jX = j\omega L = \frac{1}{j\omega C}$$

$$j\,3.636 = j(2\pi)(2e9)(L)$$

Solving for L, L = 0.289344nH

Now, only the real part of the impedance needs to be matched to 50 ohms.

The second step in constructing this network would be to find the matching Q of the circuit. The matching Q of the circuit is defined using the ratio of Rp (shunt resistance) and Rs (series resistance). In the case of the fundamental frequency, an input impedance matching circuit was designed and the values for the lumped components were calculated as follows:

$$Q^2 + 1 = \frac{Rp}{Rs} = \frac{50}{19.847}$$

$$Q = 1.23259$$

$$Q = \frac{\omega L}{R_S} = \frac{\omega C}{G_P}$$

$$L = \frac{Q\,R_S}{\omega} = \frac{(1.23259)(19.847)}{2\pi(2e9)} = 1.947e - 9 = 1.947nH$$

$$C = \frac{Q}{\omega R_P} = \frac{1.23259}{2\pi(2e9)(50)} = 1.96173e - 12 = 1.96173\,pF$$

The resulting circuit for the fundamental input side looks like the circuit shown in Fig 15.

Term
Term2
Num=2
Z=50 Ohm

C
C1
C=1.96172 pF

L
L1
L=1.94672 nH
R=

L
L2
L=0.289344 nH
R=

Term
Term1
Num=1
Z=50 Ohm

at 2 GHz

Zin = 19.847 + j 3.636
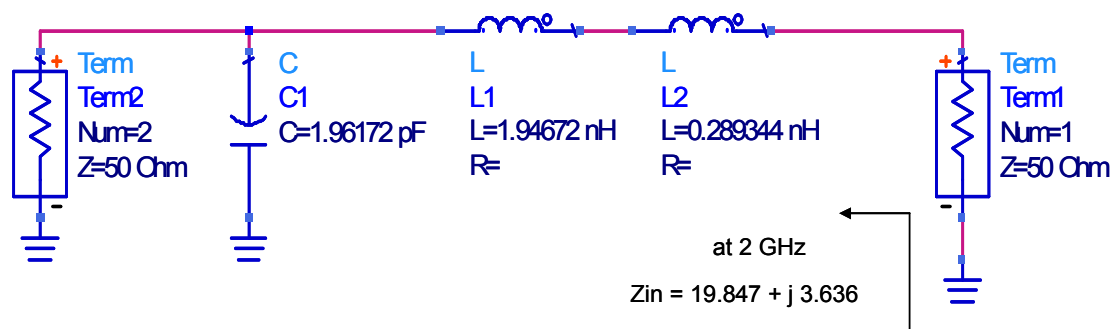
Figure 15: Input matching network at the fundamental frequency using ideal values

Similarly, in the case of second harmonic frequency, the optimum impedance was found to be 7.157 + j 53.478 Ohms. An inductor of 2.128nH was used to get rid of the reactance part of the optimum impedance value. Next the real part of the optimum impedance was matched to 50 Ohms using a Q^2+1 match. The input impedance matching circuit was designed and the values for the lumped components were calculated as follows:

$$Q^2 + 1 = \frac{Rp}{Rs} = \frac{50}{7.157}$$

$$Q = 2.444666$$

$$L = \frac{Q\,R_S}{\omega} = \frac{(2.445)(7.157)}{2\pi(4e9)} = 6.9626e - 10 = 0.69626nH$$

$$C = \frac{Q}{\omega R_P} = \frac{2.445}{2\pi(4e9)(50)} = 1.94567e - 12 = 1.94567\,pF$$

The resulting circuit using these ideal values is shown in Fig 16.
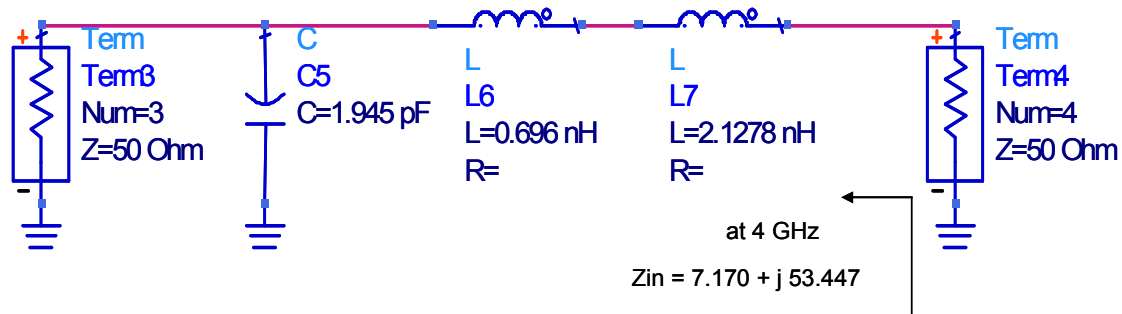
Figure 16: Input matching network at the second harmonic frequency using ideal values

In the case of the optimum load impedance, the matching network model that was used was slightly different. This model resembled Fig 17.
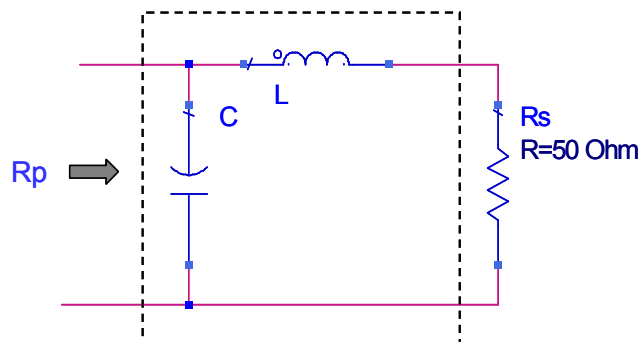
Figure 17: Simple matching network model used for load impedance matching

The load impedance was found to be 108.537 – j 10.417 ohms. A capacitor of 7.63919pF is used to get rid of the reactance part of the optimum impedance value. Next the real part of the optimum impedance was matched to 50 ohms using a Q^2+1 match. The input impedance matching circuit was designed and the values for the lumped components were calculated as follows:

$$Q^2 + 1 = \frac{Rp}{Rs} = \frac{108.537}{50}$$

$$Q = 1.082$$

$$L = \frac{Q\,R_S}{\omega} = \frac{(1.082)(50)}{2\pi(2e9)} = 4.305e-10 = 4.305nH$$

$$C = \frac{Q}{\omega R_P} = \frac{1.082}{2\pi(2e9)(108.537)} = 7.93304e-13 = 0.793304\,pF$$

The resulting circuit using these ideal values is shown in Fig 18.
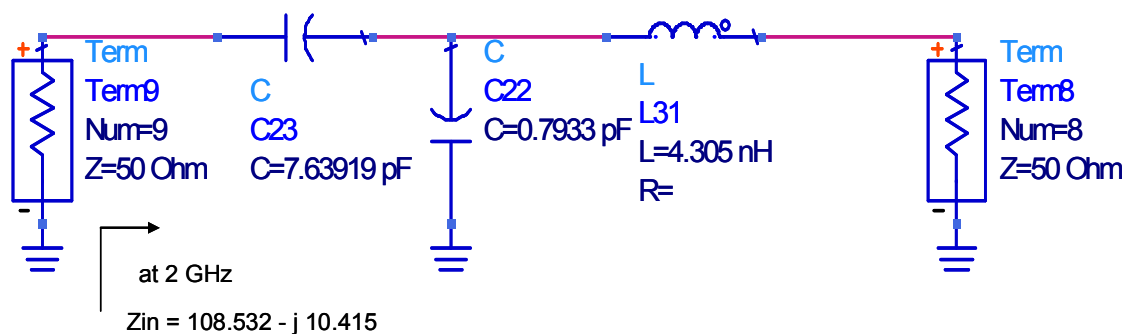
Figure 18: Output matching network at 2GHz using ideal values

The input of the device needed to be connected to a diplexer that separated the fundamental frequency from the second harmonic frequency. The fundamental frequency port of the diplexer was then connected to the circuit designed for the input matching network at the fundamental frequency as shown in Fig 15. The second harmonic port of the diplexer was connected to the circuit designed for the input matching network at the second harmonic frequency as shown in Fig 16. The diplexer design shown in Fig 10 can be used for this purpose. The diplexer consists of 8 lumped components on the fundamental frequency

side and 8 lumped component elements on the second harmonic frequency side. Lumped components do not work well at microwave frequencies due to component parasitics. As the number of circuit elements increase, the more difficult it is to match the simulated results to the measured results obtained from the physical design due to the increased level of complexity of the design. It also makes debugging harder. The solution was to construct a circuit as simple as possible. In this case, the simplest solutions was to construct a circuit that is resonant at the fundamental frequency and place it on the input matching network at the fundamental frequency side so that at the fundamental frequency, the only impedance that the device sees is the impedance that this network was designed for. This same technique is used on the input matching network at the second harmonic frequency. The resonant circuits were designed by first picking appropriate Q values. In this case, a Q value of 10 was chosen. So for circuit that is series resonant at 2 GHz, the inductor and capacitor values were calculated as follows:

For a resonant circuit,

$$\omega = \frac{1}{\sqrt{LC}}$$

For a series resonant circuit,

$$Q = \frac{\omega L_S}{R_S}$$

Therefore at 2GHz the resonant circuit inductor and capacitor values were,

$$L_S = \frac{QR_S}{\omega} = \frac{(10)(50)}{(2\pi)(2e9)} = 39.7887 \, nH$$

$$C_S = \frac{1}{\omega^2 L_S} = \frac{1}{((2\pi)(2e9))^2 (39.7887e-9)} = 0.159155e-12 = 0.159155 \, pF$$

Similarly at 4GHz the resonant circuit inductor and capacitor values were,

$$L_S = \frac{QR_S}{\omega} = \frac{(10)(50)}{(2\pi)(4e9)} = 19.89 \, nH$$

$$C_S = \frac{1}{\omega^2 L_S} = \frac{1}{((2\pi)(4e9))^2 (19.89e-9)} = 3.1831e-13 = 0.079595 \, pF$$

The resulting input matching networks with the resonant circuit is shown in Fig 19.
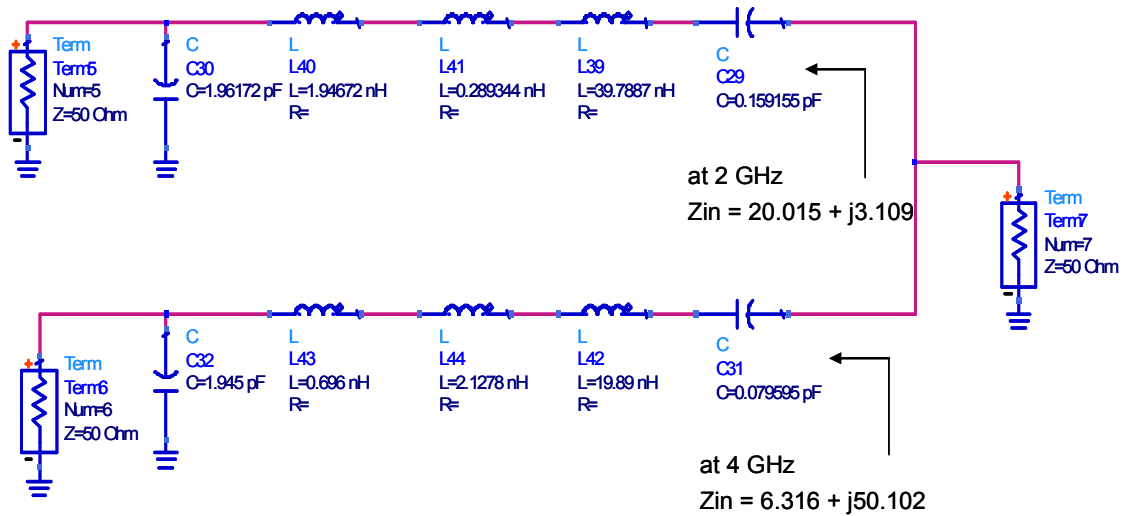
Figure 19: Input matching network

The input matching network and the output matching network circuits that are shown in Fig 19 and 18 were then modified to include the pads, parasitics and RETMA values. The parasitic models for the 0402 inductors and capacitors that were used are shown in Appendix 9 and the modified input and output matching networks is shown in Appendix 10.

3.2.4. Simulation Setup and Results for the Matching Network

Proprietary ADS device model of CRF24010 was provided by CREE. This device model was used in obtaining simulation data. The device was connected to the designed matching network at the fundamental frequency and the second harmonic frequency at the input port. The output matching network was connected to the output port. A transient simulation was run in order to look at the nonlinear analysis corresponding to the device. Since the matching networks were themselves derived from the measured S-parameters for the different sections of the load pull setup, it was decided that these measured data would be used to perform the simulations. This decision presented a problem since frequency based S-parameters cannot be used when performing transient simulations. Therefore the S-parameters devices corresponding to the test fixture, the male-to-male connectors, the couplers and the tuners were modeled with transmission line using the de-embedding technique. A diplexer model with microstrip lines that closely matches the measured data

was used for the purposes of the simulation. The overall block diagram of the simulation circuit is shown in Fig 20.
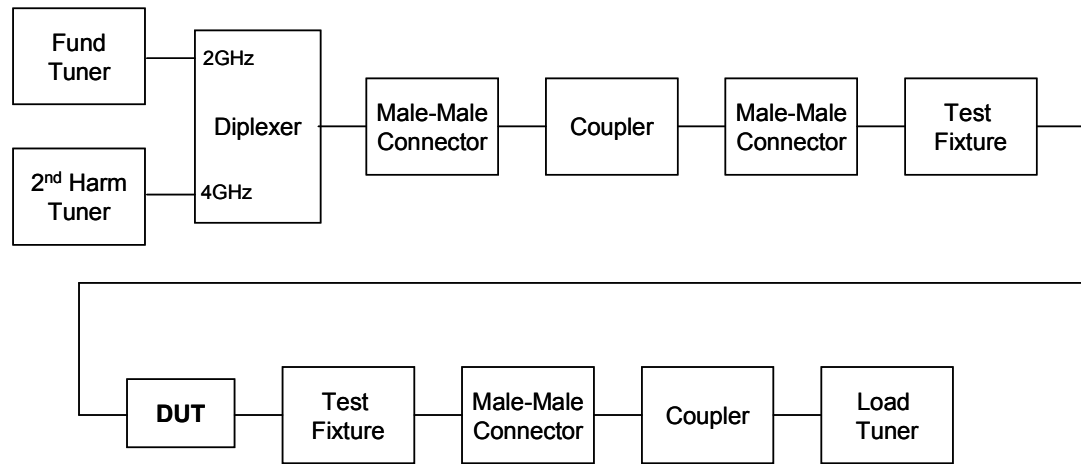
Figure 20: Block diagram of matching network setup

Appendix 11 shows the transmission line model that was used in place of each block. The fundamental source tuner and the load tuner were set at fixed optimum positions and this corresponding optimum impedance was modeled by adjusting the electrical length of the transmission line from the tuner model. The harmonic tuner, on the other hand, must be adjustable so that the second harmonic output power can be looked at as a function of second harmonic input impedance. The structure that was used to model the second harmonic input tuner is shown in Fig 21.
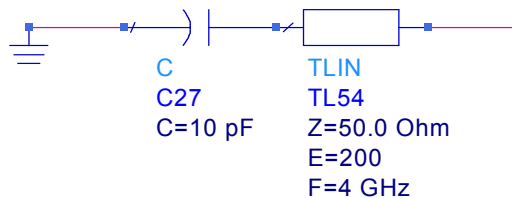
Figure 21: Second harmonic tuner modeled using transmission line

Changing the electrical length, E, of the transmission line shown in Fig 21 simulates the changes of the capacitive slug in tuner position on the actual tuner. Fig 22 shows a circuit that is used to simulate the spectrum analyzer with a second harmonic filter so that the output power at the second harmonic could be noted.
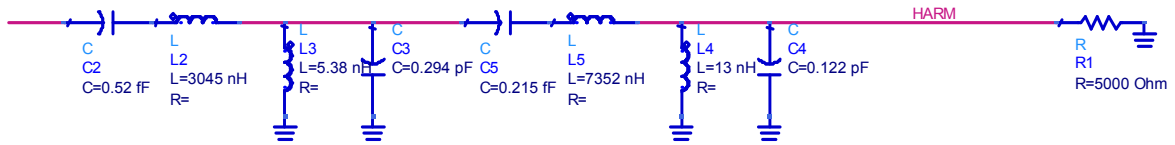
Figure 22: Model of spectrum analyzer using lumped constant elements in ADS

By changing the E of the transmission line over a predetermined range, the output power at 4 GHz can be obtained. The output voltage "HARM" seen on Fig 22 was used to arrive at the second harmonic power for the device. By taking 20 log of the output peak-to-peak voltage at HARM, the harmonic output power was obtained. This is not the absolute power, but in this case only the change in simulated second harmonic power compared to the measured second harmonic power was of interest. The electrical length of the transmission line used to model the second harmonic tuner was varied from 10 to 1000 degrees. This corresponds to change in the second harmonic input impedance as set by the tuner. The tuner positions and their corresponding impedances are tabulated and shown in Appendix 12 along with the second harmonic impedances corresponding to electrical length ranging from 10 to 1000 embedded to the input of the DUT and plotted on the Smith Chart.
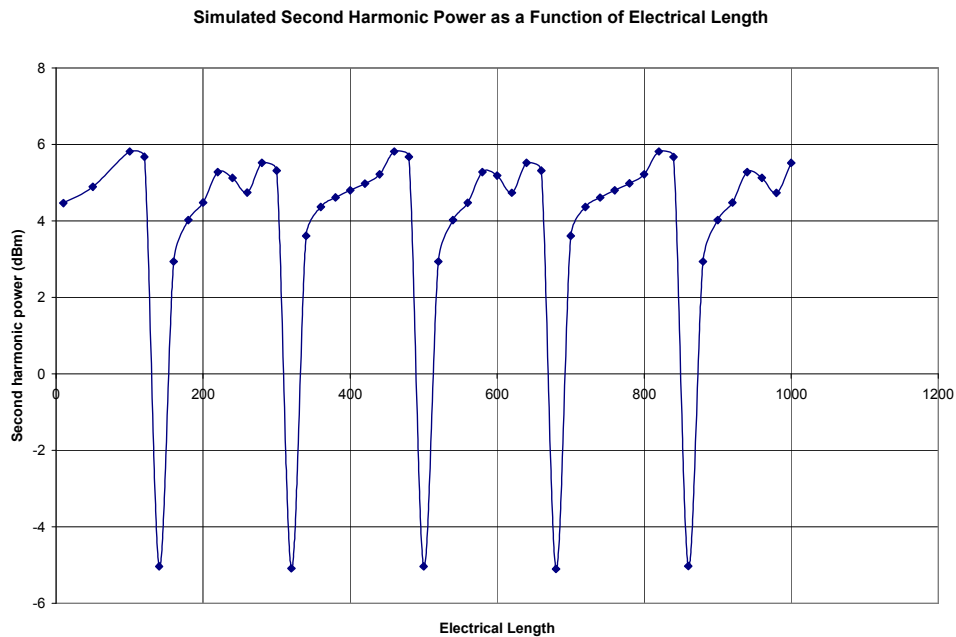
Figure 23: Simulation results for second harmonic power vs. electrical length

As the tuner position changes, the corresponding impedance of the tuner also changes. Looking at this tuner impedance on a Smith Chart, the impedance goes around the chart in a circle. The output power corresponding to these impedances that is shown in Fig 23 ranges from 5.8 to -5.1 dbm. Comapring this to the results found in Fig 13, the trend second harmonic output power trend matches very well. In the case of the measured results, the output power has approximately a 13 dB range (from 9.7 dBm to -3.2dBm) and in the case of the simulated results, the output power varies from 5.8 to -5.1 dBm, which is approximately a 11 dB range. The measured results match very closely to what was simulated.

3.2.5. Measured Results for the Matching Network Circuit

As described in earlier sections, the matching network that was designed for the device was added to the device on the gate and drain ports of the device. A picture of the complete board containing an input impedance match, an output impedance match and the device itself is shown in Appendix 13. The input and output impedances were measured before the boards were assembled together. The results are shown in Table 3.

Table 3: Ideal, simulated and measured fundamental, second harmonic, and output impedances

	Fundamental Impedance		Second Harmonic Impedance		Output Impedance	
	Real	Imaginary	Real	Imaginary	Real	Imaginary
Ideal	19.847	3.636	7.157	53.478	108.537	-10.417
Simulated	19.737	1.314	7.039	55.108	106.154	-8.054
Measured	20.922	-1.249	5.738	42.327	98.23	-10.16

After verifying that the input and output impedances matched the simulated values, the boards were put together and the device was connected to these input and output matching networks. The resulting board was then tested using the same rf power and pulse bias system as the load system but with the spectrum analyzer as the power detector. The results are presented in Table 4.

Table 4: Measured fundamental and second harmonic output power results

	Fundamental Output Power	Second Harmonic Output Power
Using Automated Tuners	32.5 dBm	9.5 dBm
Using Matching Network	29.6 dBm	11.4 dBm

Looking at table 14, there is a slight difference between the second harmonic power that was measured using the automated tuners and the second harmonic power that was measured using the designed input and output matching networks. This loss of about 3dB can partially be attributed to higher PCB losses in the system than with the very low loss load pull system.

CHAPTER 4. SUMMARY AND CONCLUSIONS

The design of nonlinear devices using CAD tools with a nonlinear model of the device has gained importance in recent times, but the accuracy of such models is questionable especially when these CAD tools are used to simulate the nonlinear operation of the device at the fundamental frequency as well as harmonic frequencies under different biasing conditions [12]. Experimental measurements provide accurate data about the nonlinear device. Most experimental techniques used to design power amplifiers only take the fundamental frequency into account while ignoring the harmonic effects. When design constraints are stringent in terms of output power and efficiency, harmonic effects need to taken into account by the designer if the specifications are to be met. The load pull system is an important measurement technique used in making large signal nonlinear device operation measurements both at the fundamental frequency as well as the harmonic frequencies under different biasing conditions [12].

Power MESFET devices like the one tested can be used to design power amplifiers with the measurements that are already collected. By finding the input and output impedances that would result in the best device circuit performance as well as maximum or minimum second harmonic effects, high efficiency power amplifiers can be designed. These types of power amplifiers can be used in communication circuits, especially as part of the transmitter circuit. The power amplifier is the largest source of distortion in wireless communication circuits. Therefore it is very important to design the power amplifier for best performance [13]. This can be done by characterizing the device itself at both fundamental as well as harmonic frequencies. In this research project the second harmonic effects are studied and the circuit performance is optimized by controlling the second harmonic input impedance.

For the purposes of this research project, the load pull system is used make second harmonic measurement in order to examine the second harmonic effects on the output power of a SiC power MESFET device (CREE CRF24010) at 2 GHz and a Vds of 25V, Ids of 530mA under a pulsed rf and pulsed bias condition with a 1% duty cycle. The second harmonic input impedance was varied using automated tuners and the corresponding output power at the second harmonic frequency (4 GHz) was measured. Depending on the second

harmonic input impedance, the output power varied from 9.5 dBm to 11.4 dBm. In this case, the measured data was used to design input and output matching network circuits on PCB that would provide the maximum second harmonic output power. The matching network circuits were then connected to the DUT and it was verified that the DUT still provided the same output power at the fundamental and second harmonic frequencies as when the measurements were made with the automated tuner. This means that the matching networks that were designed could be utilized whenever the DUT is used in a circuit that requires the best performance from the DUT. So by just adding the matching networks to the input and output of the DUT, the device has been made efficient and thus the circuit that the DUT is used in will only see the best performance from the DUT.

APPENDIX 1: PICTURE OF THE LOAD PULL SETUP
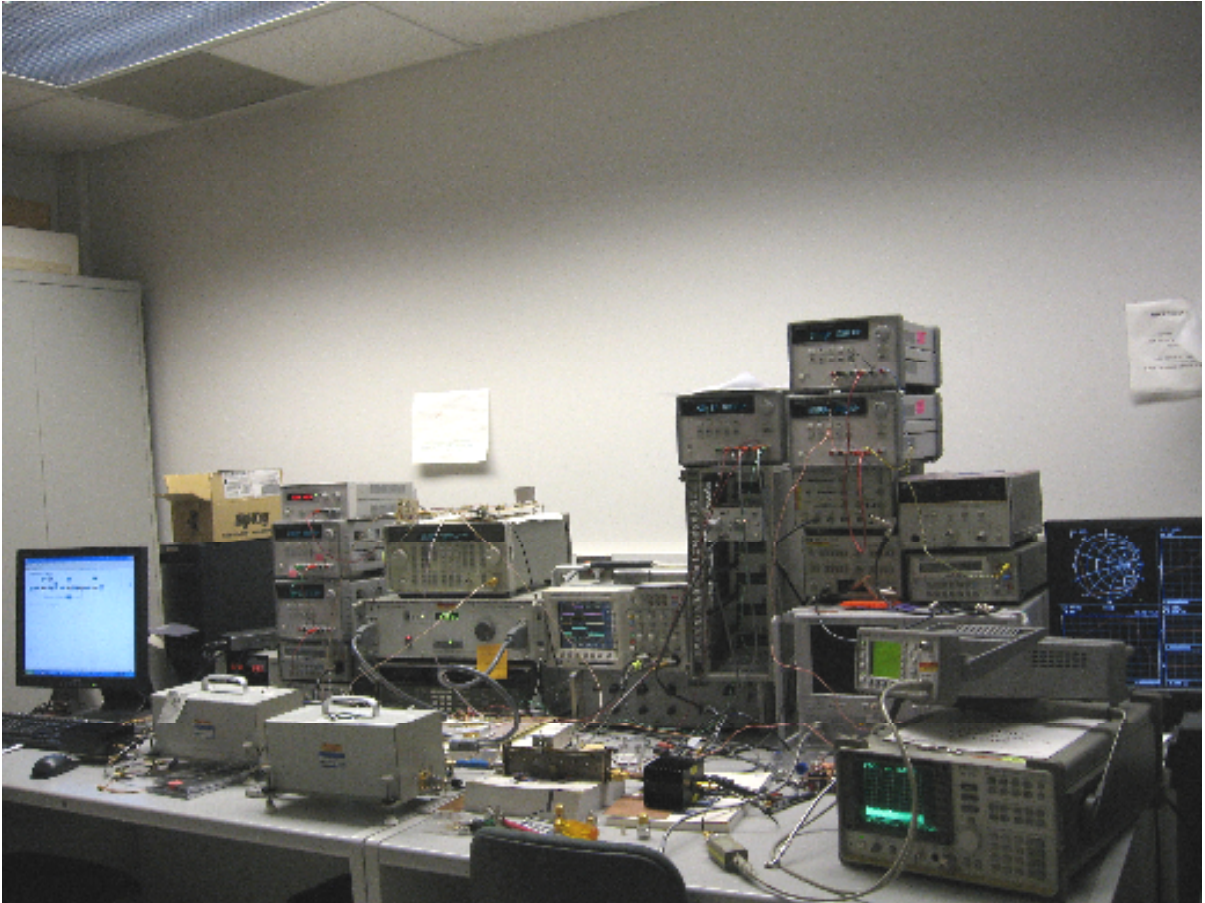
APPENDIX 2. LOAD PULL RESULTS FOR SiC MESFET DEVICE AT 2.0GHz USING SNPW PROGRAM
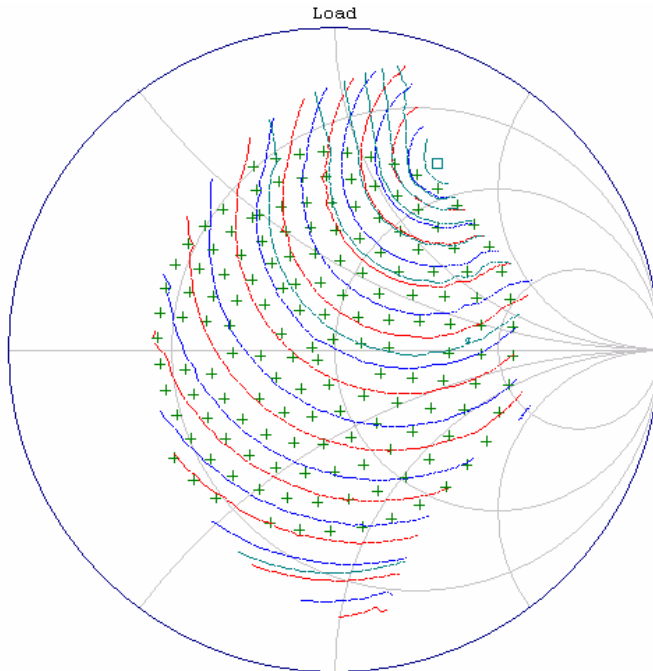
Load

Fixed Load Pull
Freq = 2.0000 GHz
ZSource (Ohms): 2.33 + j 2.78

Pout   max = 31.92 dBm
  at 3.58 + j 7.21 Ohms
10 contours, 2.00 dBm step
(12.00 to 30.00 dBm)
Gt   max = 19.04 dB
  at 3.58 + j 7.21 Ohms
10 contours, 2.00 dB step
(0.00 to 18.00 dB)
Eff   max = 11.12 %
  at 3.58 + j 7.21 Ohms
10 contours, 1.50 % step
(-3.00 to 10.50 %)
Specs: OFF

Zload (Ohms) @ 3.79 + j 6.37

Pin_avail = 12.877 dBm
Pout   = 31.155 dBm
Gt   = 18.277 dB
Eff   = 9.726 %
V_out   = 24.991 V
I_out   = 528.000 mA
V_in   = 9.158 V
I_in   = 2.010 mA
Drain_eff = 9.873 %

APPENDIX 3. EMBEDDING FUNDAMENTAL INPUT IMPEDANCE TO THE GATE OF THE DUT
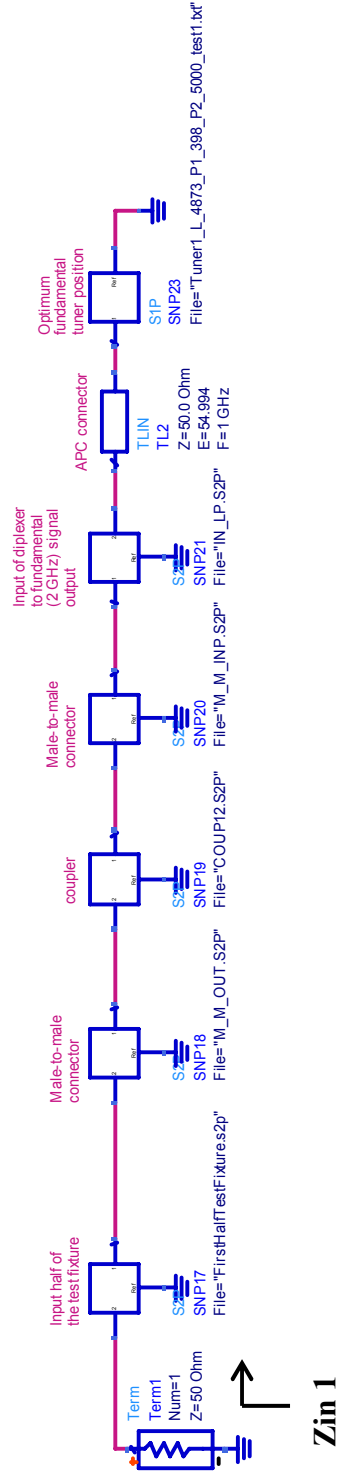
freq	Zin1
2.000 GHz	19.847 + j3.636

APPENDIX 4. EMBEDDING SECOND HARMONIC INPUT IMPEDANCE TO THE GATE OF THE DUT
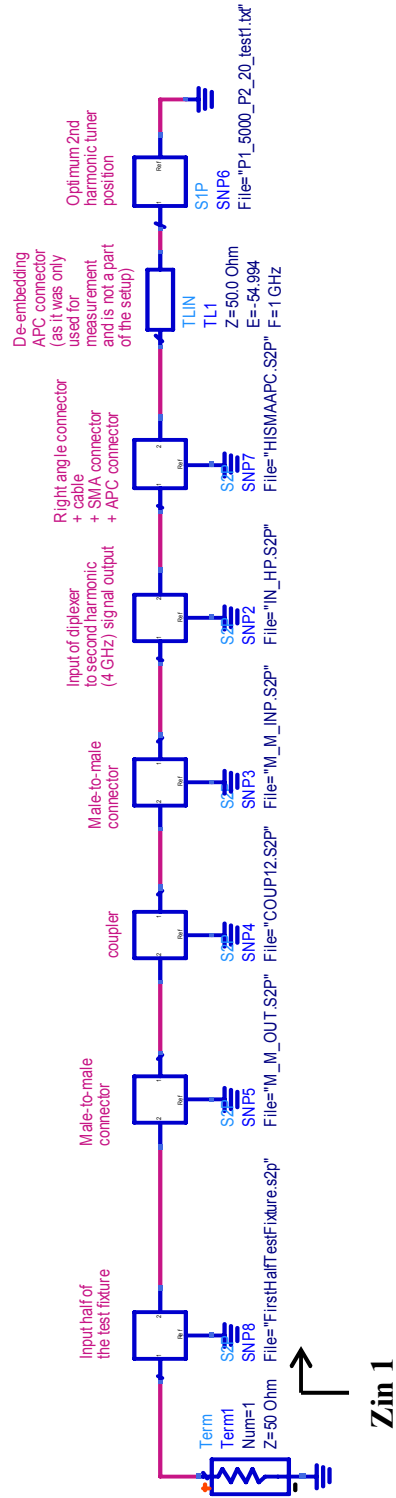
freq	Zin1
4.000 GHz	7.157 + j53.478

APPENDIX 5. EMBEDDING OUTPUT IMPEDANCE TO THE DRAIN OF THE DUT
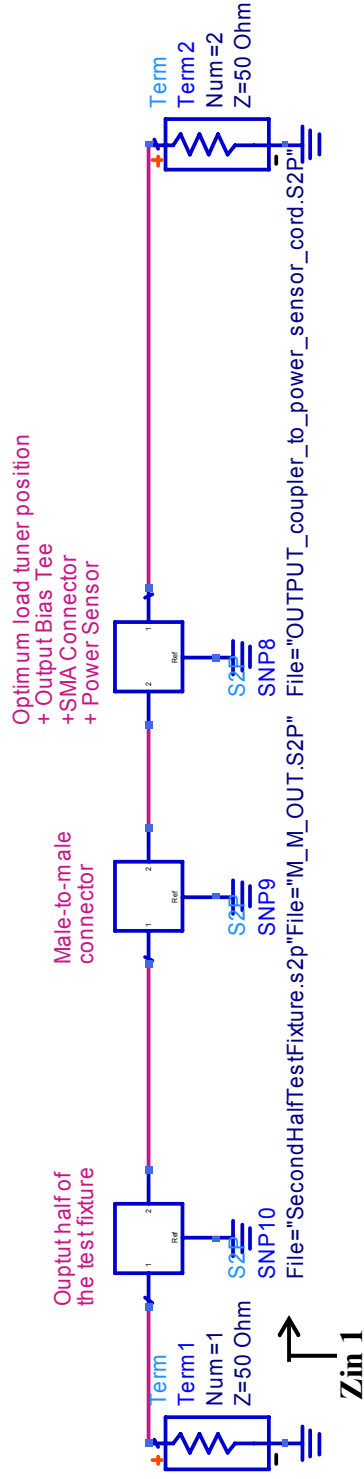
freq	Zin1
2.000 GHz	108.537 - j10.417

APPENDIX 6. TEST FIXTURE S-PARAMETER CALCULATIONS

When making s-parameter measurements on the test fixture, the measurements were made for the fixture as a whole. Since the Maury SNP program requires that the s-parameter on port 1 of the DUT be input as one file and the s-parameter on port 2 of the DUT be input as another file, the s-parameter for each half of the DUT needs to be derived from the complete fixture s-parameter file that was measured.

The two halves of the fixture are to be called Part A and Part B from now onwards. Fig 24 shows the two parts of the fixture whose s-parameters are to be measured. Part A and part B of the fixture are assumed to be symmetrical. So the assumption that port 2 of part A and port 2 of part B are the same is made.
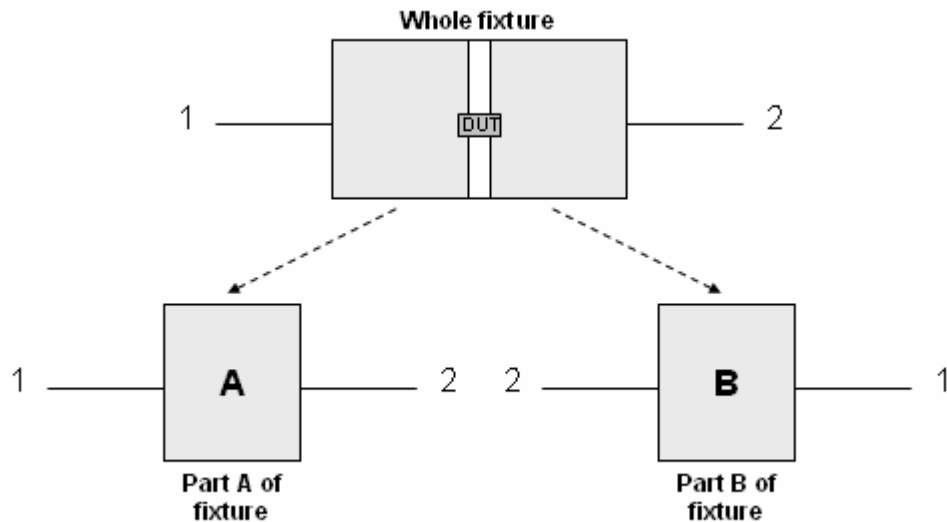
Figure 24: Test fixture setup

The s-parameter of the whole fixture is known from the measured results and the s-parameters of part A and part B is to be derived from the measured s-parameter file of the whole fixture. Fig 25 gives an overview of the process used to perform this derivation. The s-parameter of the whole fixture is converted to T-parameters. From this, the corresponding T-parameters from part A and part B is calculated. Once the T-parameters have been obtained, they are once again converted back to s-parameters for part A and part B. This is the overall process.
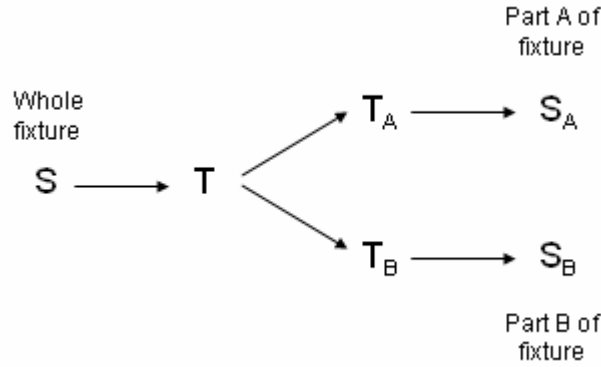
Figure 25: Overview of the derivation process

The first step in finding the s-parameters for each part is to convert the s-parameter for the whole fixture to T-parameters. This is done using the Gonzalez method as shown in (27) [11].

$$(T)\big|_G = \begin{pmatrix} \dfrac{1}{S_{21}} & -\dfrac{S_{22}}{S_{21}} \\ \dfrac{S_{11}}{S_{21}} & -\dfrac{\Delta s}{S_{21}} \end{pmatrix} \tag{27}$$

Since, from an earlier assumption, it is known that part A is symmetrical to part B, the T-parameters for these two parts are as follows:

T-parameter for part A $= \begin{pmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{pmatrix}$ \hfill (28)

T-parameter for part B $= \begin{pmatrix} T_{11} & -T_{21} \\ -T_{12} & T_{22} \end{pmatrix} \cdot \dfrac{1}{\Delta T}$ \hfill (29)

The T-parameters for the whole fixture is assumed to be as follows:

$$T_{total} = \begin{pmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{pmatrix} \tag{30}$$

The product of the T-parameters from part A and part B results in the T-parameter for the whole fixture. This is shown using Eqns 31 and 32.

$$\begin{pmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{pmatrix} \begin{pmatrix} T_{11} & -T_{21} \\ -T_{12} & T_{22} \end{pmatrix} \cdot \dfrac{1}{\Delta T} = T_{total} \tag{31}$$

$$\frac{1}{\Delta T}\begin{pmatrix} T_{11}{}^2 - T_{12}{}^2 & -T_{11}T_{21} + T_{12}T_{22} \\ T_{11}T_{21} - T_{12}T_{22} & T_{22}{}^2 - T_{21}{}^2 \end{pmatrix} = T_{total} = \begin{pmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{pmatrix} \tag{32}$$

Since $\Delta T = T_{11}T_{22} - T_{12}T_{21} = 1 + j0$ and $G_{21} = - G_{12}$,

$$T_{11}{}^2 - T_{12}{}^2 = G_{11} \tag{33}$$

$$-T_{11}T_{12} + T_{12}T_{22} = G_{12} \tag{34}$$

$$T_{11}T_{12} - T_{12}T_{22} = -G_{12} \tag{35}$$

$$T_{22}{}^2 - T_{12}{}^2 = G_{22} \tag{36}$$

Since $\Delta T = 1$, we also know that

$$T_{11}T_{22} + T_{12}{}^2 = 1 \tag{37}$$

$$1 - T_{11}T_{22} = T_{12}{}^2 \tag{38}$$

From (35),

$$T_{12} = -G_{12} / (T_{11} - T_{22}) \tag{39}$$

(33) – (36) results in (40):

$$T_{11}{}^2 - T_{22}{}^2 = G_{11} - G_{22} = (T_{11} - T_{22})(T_{11} + T_{22}) \tag{40}$$

(33) + (36) results in (41):

$$T_{11}{}^2 - 2\,T_{12}{}^2 + T_{22}{}^2 = G_{11} + G_{22} \tag{41}$$

$$T_{11}{}^2 - 2(1 - T_{11}T_{22}) + T_{22}{}^2 = G_{11} + G_{22} \tag{42}$$

$$T_{11}{}^2 + 2T_{11}T_{22} + T_{22}{}^2 - 2 = G_{11} + G_{22} \tag{43}$$

$$(T_{11} + T_{22})^2 = G_{11} + G_{22} + 2 \tag{44}$$

From the previous simplifications,

$$(T_{11} + T_{22})^2 = G_{11} + G_{22} + 2 \tag{45}$$

$$T_{11}{}^2 - T_{22}{}^2 = G_{11} - G_{22} \tag{46}$$

If,

$$A = T_{11} + T_{22} \tag{47}$$

$$B = T_{11} - T_{22} \tag{48}$$

Then,

$$A^2 = G_{11} + G_{22} + 2 \tag{49}$$

$$AB = G_{11} - G_{22} \tag{50}$$

$$A = \pm\sqrt{G_{11} + G_{22} + 2} = T_{11} + T_{22} \tag{51}$$

$$B = \mp \frac{G_{11} - G_{22}}{\sqrt{G_{11} + G_{22} + 2}} = T_{11} - T_{22} \tag{52}$$

$$T_{11} = \frac{A + B}{2} \tag{53}$$

$$T_{22} = \frac{A - B}{2} \tag{54}$$

$$T_{12} = -\frac{G_{12}}{B} \tag{55}$$

$$T_{21} = -T_{12} = \frac{G_{12}}{B} \tag{56}$$

$$(S_A) = \begin{pmatrix} \dfrac{T_{21}}{T_{11}} & \dfrac{\Delta T}{T_{11}} \\ \dfrac{1}{T_{11}} & -\dfrac{T_{12}}{T_{11}} \end{pmatrix} \tag{57}$$

$$(S_B) = \begin{pmatrix} \dfrac{T_{21}}{T_{11}} & -\dfrac{1}{T_{11}} \\ -\dfrac{1}{T_{11}\Delta T} & -\dfrac{T_{12}}{T_{11}} \end{pmatrix} \tag{58}$$

APPENDIX 7: INPUT IMPEDANCE AT THE TUNER AND DUT PLOTTED ON A SMITH CHART

The impedance circles shown in this appendix contain both blue and red impedance circles. The red circle corresponds to the impedance at the tuner and the blue circle corresponds to the impedance at the DUT (after embedding is completed). On the smith chart, m1 and m3 correspond to the impedance that provides the maximum second harmonic output power and m2 and m4 correspond to the impedance that provides the minimum second harmonic output power.

At tuner positions: P1 = 5000, P2 = 20:
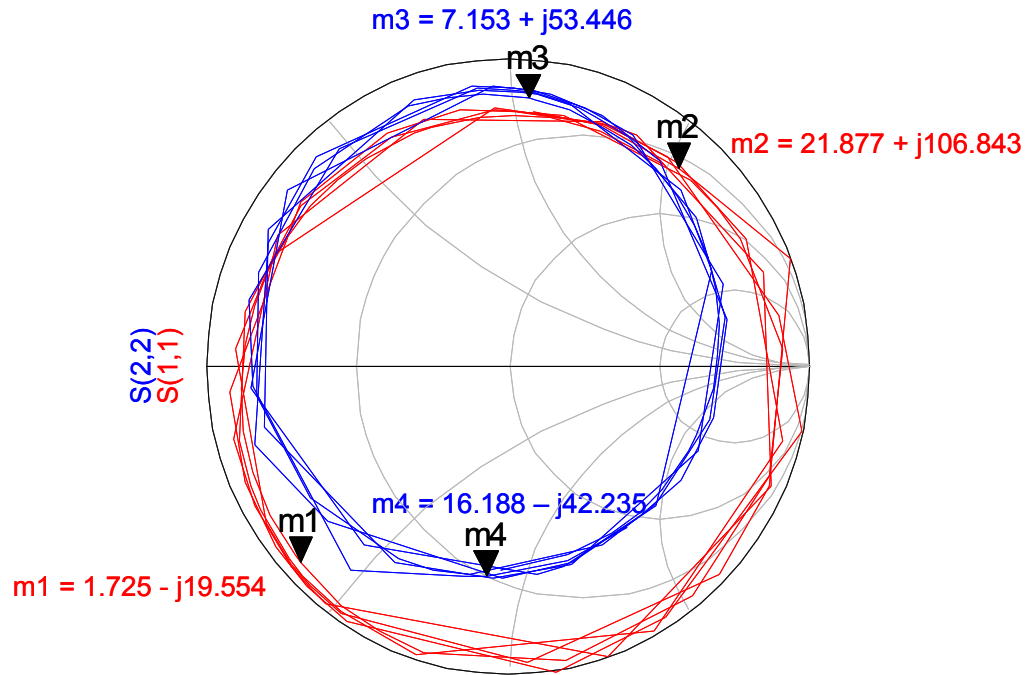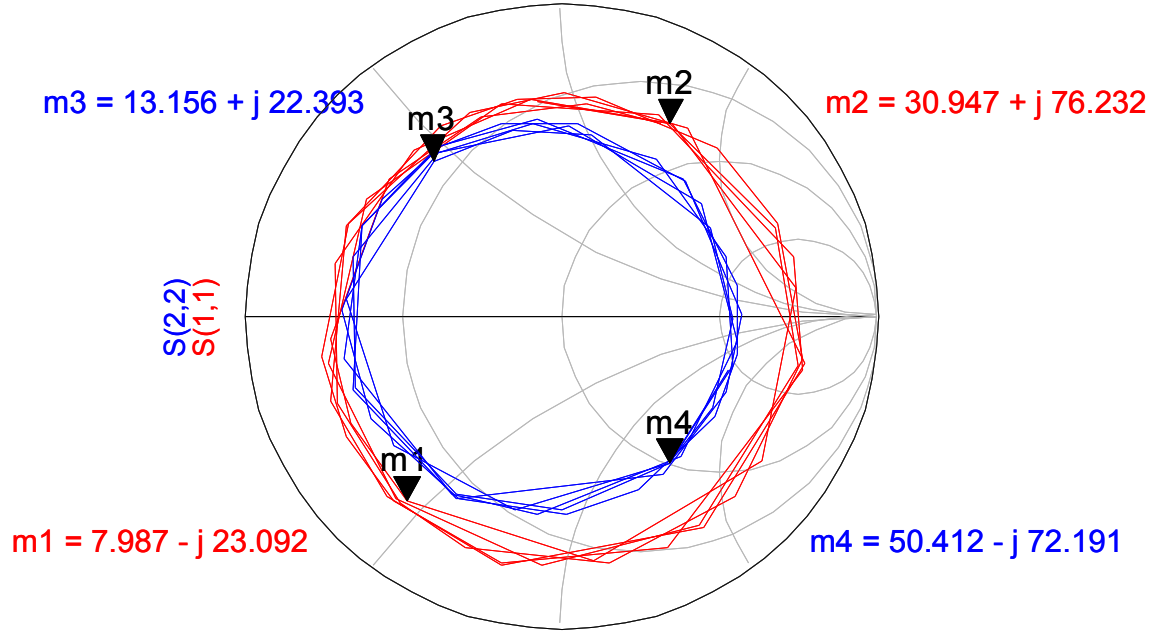
m3 = 7.153 + j53.446

m2 = 21.877 + j106.843

S(2,2)
S(1,1)

m4 = 16.188 – j42.235

m1 = 1.725 - j19.554

At tuner positions: P1 = 5000, P2 = 250:

m3 = 13.156 + j 22.393

m2 = 30.947 + j 76.232

S(2,2)
S(1,1)

m1 = 7.987 - j 23.092

m4 = 50.412 - j 72.191

At tuner positions: P1 = 5000, P2 = 500:

m2 = 55.932 + j83.858

m3 = 18.285 + j23.155

S(2,2)
S(1,1)

m1 = 12.154 – j20.234

m4 = 41.992 - j 55.712

At tuner positions: P1 = 5000, P2 = 1000:

m2 = 58.618 + j53.214

m3 = 28.269 + j19.472

S(2,2)
S(1,1)

m1 = 21.698 - j16.554

m4 = 54.549 - j 42.336

At tuner positions: P1 = 5000, P2 = 1500:

m3 = 32.809+ j10.066

m2 = 72.204+ j31.281

S(2,2)
S(1,1)

m1 = 30.906 – j15.351
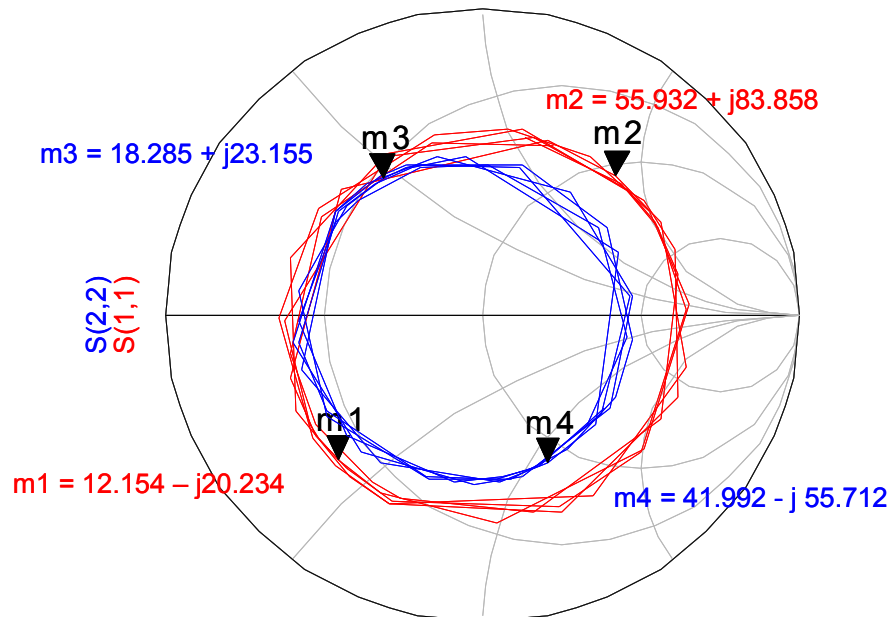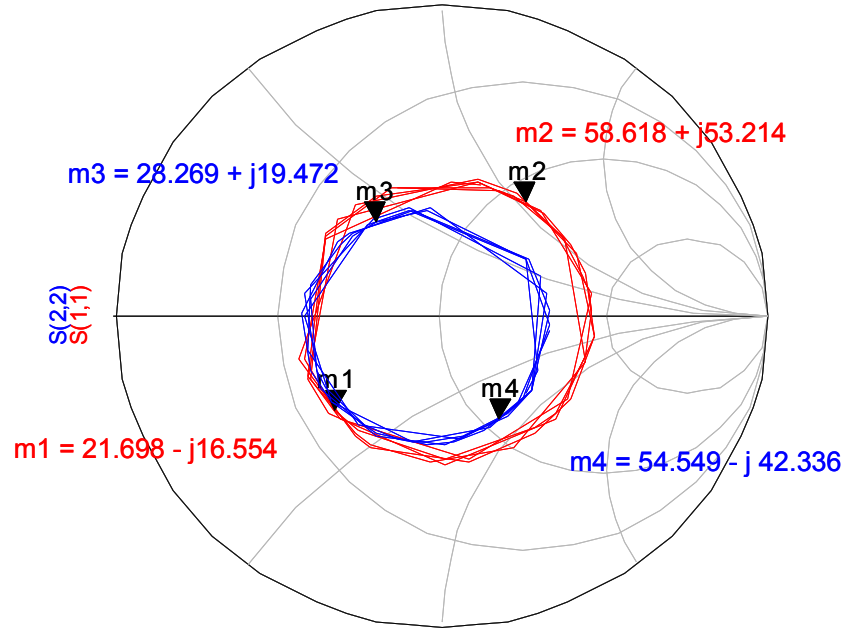
m4 = 48.200 + j27.890
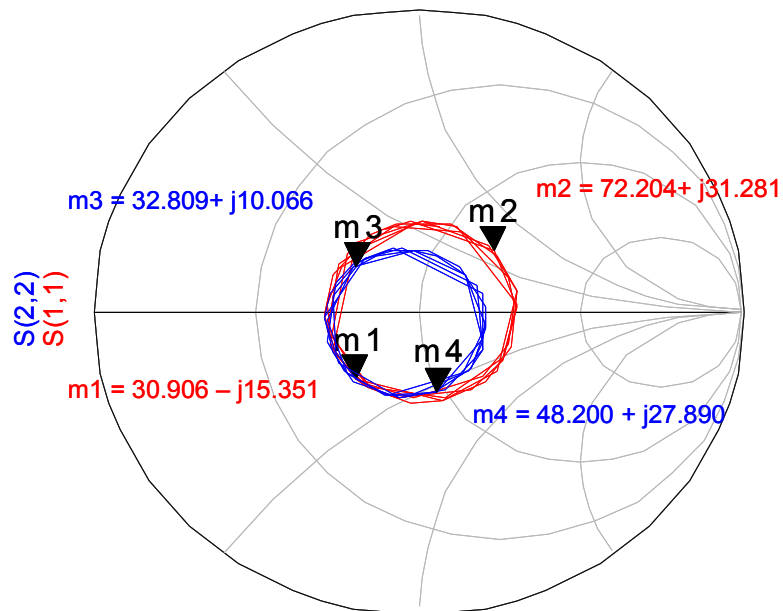
APPENDIX 8: 2nd HARMONIC INPUT IMPEDANCE CORRESPONDING TO VARIOUS TUNER POSITIONS AND OUTPUT 2nd HARMONIC POWER

Tuner Position			Impedance at Tuner		Impedance at DUT		2nd harmonic power
P1	P2	L	Real	Imaginary	Real	Imaginary	
5000	20	50	22.249	98.917	18.44018	-44.54965	-3
5000	20	250	15.081	71.769	28.1641	-59.98261	-2.8
5000	20	400	11.783	57.867	40.28787	-74.87953	-2.6
5000	20	500	10.164	50.283	53.00834	-86.90707	-2.3
5000	20	600	8.917	43.712	72.19982	-100.111	-1.9
5000	20	750	7.453	35.539	120.1856	-117.0503	-1.4
5000	20	800	7.032	32.889	146.5	-118.4027	-0.9
5000	20	950	5.992	25.723	247.6264	-66.29118	-0.3
5000	20	1050	5.397	21.398	276.2808	36.96583	0.2
5000	20	1150	4.848	17.266	222.5055	129.54425	0.9
5000	20	1250	4.374	13.198	143.5297	156.50049	1.7
5000	20	1350	3.957	9.375	89.86286	146.88159	2.5
5000	20	1450	3.563	5.662	57.80703	129.11441	3.4
5000	20	1550	3.209	1.874	38.2498	111.20407	4.4
5000	20	1650	2.872	-2.074	25.92871	95.330162	5.4
5000	20	1750	2.561	-5.895	18.44156	82.773589	6.6
5000	20	1850	2.257	-9.79	13.44964	72.32988	7.7
5000	20	1950	2.011	-14.099	9.957513	62.900897	8.8
5000	20	2050	1.763	-18.644	7.51813	54.866481	9.4
5000	20	2070	1.725	-19.554	7.152563	53.445584	9.5
5000	20	2200	1.392	-25.706	5.184349	45.170789	9.4
5000	20	2300	1.268	-31.123	4.240568	39.356847	8.7
5000	20	2400	1.088	-37.206	3.503606	34.055085	7.8
5000	20	2700	1.133	-60.87	2.632019	20.669647	4.4
5000	20	3000	4.742	-105.528	3.074507	8.8415563	1.6
5000	20	3300	40.219	-246.615	4.339804	-2.833524	-0.5
5000	20	3600	749.551	488.956	6.53212	-14.54059	-1.8
5000	20	3900	52.533	186.548	10.52352	-27.82197	-2.7
5000	20	4000	34.778	144.301	12.51575	-33.24813	-2.9
5000	20	4100	25.267	116.305	15.04789	-39.31205	-3
5000	20	4500	11.167	61.503	34.71034	-71.91245	-2.7
5000	20	4700	8.407	46.564	60.81304	-97.36993	-2.2
5000	20	5000	5.785	30.012	188.3324	-123.2033	-1
5000	20	5300	4.11	16.704	217.9701	152.08222	3.9
5000	20	5600	2.882	4.974	50.06418	129.11913	3.5
5000	20	5900	1.854	-6.717	15.31418	81.166614	6.9

5000	20	6000	1.558	-10.923	10.89578	70.134685	8
5000	20	6050	1.425	-13.119	9.283425	65.266114	8.6
5000	20	6175	1.133	-18.662	6.49688	55.06997	9.5
5000	20	6220	1.032	-20.692	5.782206	51.945195	9.7
5000	20	6330	0.777079	-26.183	4.377401	44.729808	9.5
5000	20	6500	0.467197	-36.255	3.072112	34.878324	7.9
5000	20	7000	1.097	-85.467	2.440834	12.968425	2.4
5000	20	7500	80.543	-363.478	4.50157	-6.049147	-1.1
5000	20	8000	47.237	192.452	9.802041	-27.72412	-2.9
5000	20	8270	19.453	104.287	16.12322	-43.6027	-3.2
5000	20	8500	12.144	71.829	26.02785	-61.98754	-3
5000	20	9000	6.125	35.106	123.4308	-129.3653	-1.6
5000	20	9500	3.425	12.994	137.7727	172.77139	1.6
5000	20	10000	1.557	-6.366	14.79334	82.593915	6.9
5000	20	10150	1.124	-12.608	8.904611	66.551741	8.6
5000	20	10300	0.696433	-19.224	5.638939	54.304061	9.8
5000	20	10360	0.585477	-22.165	4.815782	49.937028	9.9
5000	20	10400	0.467679	-24.326	4.28218	47.070467	9.8
5000	20	11000	-0.26718	-70.489	2.060851	17.197047	3.3
5000	20	11500	22.983	-232.074	3.753392	-2.108588	-0.6
5000	20	12000	81.097	262.893	8.406185	-23.07554	-2.7
5000	20	12500	14.364	83.931	20.69325	-53.23502	-3.1
5000	20	12570	12.643	74.616	24.5247	-59.64706	-3
5000	20	13000	6.754	70.723	82.39892	-115.4233	-2
5000	20	13500	3.747	17.034	230.4702	157.8378	0.8
5000	20	14000	1.843	-2.311	21.50609	96.549793	5.7
5000	20	14200	1.256	-10.404	10.5195	71.648697	8
5000	20	14350	0.806477	-16.872	6.508277	58.25612	9.5
5000	20	14450	0.534121	-21.648	4.846388	50.695857	9.8
5000	20	14560	0.254081	-27.301	3.628807	43.535017	9.4
5000	20	15000	-0.52048	-58.763	1.961358	21.601268	4.5
5000	20	16000	217.338	449.742	6.876973	-17.99492	-2.4
5000	20	16500	18.133	99.268	16.97213	-45.49885	-3.2
5000	20	16700	12.407	71.743	26.25305	-61.80741	-3
5000	20	17000	7.954	46.884	58.82675	-98.12543	-2.5
5000	20	18000	2.386	1.466	33.02104	112.17805	4.4
5000	20	18400	1.208	-14.606	8.128842	62.37928	8.9
5000	20	18500	0.949337	-19.064	6.090628	54.527125	9.5
5000	20	18560	0.793532	-21.865	5.172809	50.349464	9.7
5000	20	18650	0.598054	-26.336	4.148583	44.619564	9.4
5000	20	19500	4.329	-124.142	2.915177	6.0994933	0.7
5000	20	20000	1.097	276.432	5.042428	-24.07929	-2
5000	20	20500	25.547	119.948	14.42011	-38.40933	-3.1

5000	20	20560	21.877	106.843	16.18847	-42.23527	-3.2
5000	20	20800	13.454	72.083	26.74409	-60.78811	-3
5000	20	21000	9.926	54.081	44.29726	-82.16681	-2.7
5000	250	50	30.206	72.446	33.66613	-48.10958	-2.3
5000	250	300	20.048	51.985	55.63244	-64.06718	-1.9
5000	250	650	13.257	32.051	130.2636	-66.55876	-0.6
5000	250	1000	9.895	16.936	167.0725	65.169531	1.2
5000	250	1750	7.581	-11.913	22.53094	62.218352	6.8
5000	250	2000	7.987	-23.092	13.95633	45.857393	7.6
5000	250	2500	13.134	-55.216	8.114436	22.037608	4.3
5000	250	3500	293.687	124.79	12.37056	-15.18335	-1.6
5000	250	4140	30.712	76.554	30.95675	-46.93363	-2.3
5000	250	4600	15.084	41.054	85.10751	-76.22195	-1.4
5000	250	5000	10.251	21.709	189.8893	11.949119	0.4
5000	250	5800	7.014	-9.393	24.74606	67.760769	6.6
5000	250	6100	7.256	-22.721	13.30497	46.696683	7.7
5000	250	6300	8.054	-32.937	9.961687	36.245521	6.9
5000	250	6650	12.863	-58.818	7.492504	20.63149	3.9
5000	250	7000	33.548	-107.637	7.511754	7.3188338	1.3
5000	250	7800	117.432	158.761	15.03321	-23.50294	-2.1
5000	250	8085	42.813	98.683	22.79309	-37.89808	-2.3
5000	250	8500	18.982	54.637	50.5568	-65.25247	-2
5000	250	8750	13.707	38.985	94.44525	-80.34146	-1.3
5000	250	9000	10.684	26.633	176.4119	-44.44131	-0.1
5000	250	9900	6.477	-8.8823	24.36632	69.614213	6.5
5000	250	10180	6.635	-21.027	13.46877	49.152223	7.8
5000	250	10500	8.045	-38.907	8.400442	31.758706	6.2
5000	250	11000	21.847	-89.286	6.928268	11.237531	2.1
5000	250	11500	253.366	-196.432	9.451974	-7.130618	-0.8
5000	250	12300	32.634	83.509	27.37006	-44.38912	-2.5
5000	250	12700	16.422	47.824	63.93956	-72.69667	-1.8
5000	250	13000	11.665	31.268	141.7804	-72.27093	-0.7
5000	250	13500	7.914	10.354	110.6603	109.41489	2.3
5000	250	13880	6.674	-4.093	33.52595	80.583582	5.5
5000	250	14100	6.492	-13.101	19.29655	61.341589	7.2
5000	250	14300	6.737	-21.947	13.09353	47.940621	7.8
5000	250	14600	8.307	-38.739	8.619748	31.824324	6.3
5000	250	15000	16.846	-74.758	7.005624	15.047888	2.8
5000	250	15580	223.365	-200.094	9.350609	-6.337963	-0.7
5000	250	15900	195.077	175.566	13.18585	-18.99543	-1.8
5000	250	16500	26.933	71.744	33.40132	-50.65575	-2.3
5000	250	17000	13.344	36.118	108.4702	-78.19383	-1
5000	250	18000	7.054	-4.992	32.5255	77.52212	5.6

5000	250	18400	7.201	-21.957	13.66399	47.684104	7.7
5000	250	18800	10.056	-45.266	8.338735	27.415692	5.4
5000	250	19200	23.653	-87.393	7.446416	11.485458	2.1
5000	250	19700	236.834	-181.452	9.872671	-6.705446	-0.8
5000	250	20100	125.567	154.617	15.34092	-22.78496	-1.9
5000	250	20560	30.947	76.232	31.16636	-46.7873	-2.3
5000	250	21000	15.778	42.043	81.05329	-74.2098	-1.4
5000	500	50	35.457	60.514	43.77924	-44.27867	-1.8
5000	500	500	19.654	34.107	101.1385	-49.00504	-0.8
5000	500	1000	13.534	13.456	122.4102	59.319443	1.5
5000	500	1500	11.787	-4.735	42.36597	67.182111	4.6
5000	500	1750	12.153	-14.586	26.16841	52.724429	5.9
5000	500	2000	13.678	-25.764	18.04999	39.77545	6.2
5000	500	2100	14.768	-30.883	16.03868	35.116417	5.9
5000	500	3000	93.836	-109.817	12.46887	1.5180309	0.5
5000	500	3500	181.913	81.376	17.76434	-16.09031	-1.3
5000	500	3700	100.637	100.242	22.15152	-24.1276	-1.8
5000	500	3850	67.453	88.707	26.65039	-30.36509	-1.9
5000	500	4250	30.503	55.467	49.78048	-48.57937	-1.8
5000	500	4800	16.234	26.133	135.2705	-24.23786	-0.1
5000	500	5500	11.488	-0.575013	53.54732	74.423403	4
5000	500	5850	11.587	-14.134	25.99182	53.989168	6
5000	500	5900	11.766	-16.209	23.88525	51.164536	6.2
5000	500	5990	12.154	-20.234	20.57844	46.196861	6.4
5000	500	6150	13.441	-27.805	16.64193	38.208652	6.1
5000	500	7000	63.22	-101.077	11.51512	5.2769647	0.6
5000	500	7500	230.304	29.124	15.62605	-12.27935	-1.2
5000	500	7850	88.654	101.232	22.6679	-26.16109	-1.8
5000	500	8130	43.984	73.786	33.71456	-39.09892	-1.9
5000	500	8450	25.583	49.675	59.09941	-53.97787	-1.5
5000	500	9200	12.657	14.45	132.1107	60.389579	1.4
5000	500	9600	10.863	-0.324748	53.40928	76.909783	4
5000	500	10000	11.018	-16.054	23.11771	52.152799	6.3
5000	500	10100	11.458	-20.442	19.66026	46.546527	73.5
5000	500	10300	13.021	-30.037	15.1408	36.640935	6.1
5000	500	10800	26.866	-65.843	10.93154	16.10422	2.8
5000	500	11300	126.075	-122.486	12.22767	-1.490274	0
5000	500	11800	143.666	107.06	18.73174	-19.82	-1.6
5000	500	12000	77.258	97.814	23.87346	-28.28417	-2
5000	500	12500	27.318	53.102	53.40465	-52.20945	-1.8
5000	500	13500	11.509	7.134	87.79301	82.320983	2.5
5000	500	14000	10.801	-11.817	27.90703	58.238521	5.8
5000	500	14260	11.885	-23.026	18.20177	43.53197	6.3

5000	500	14400	13.083	-30.153	15.13531	36.528665	6
5000	500	15000	34.267	-76.113	10.94369	12.506204	2.1
5000	500	15500	178.679	-107.094	13.1497	-4.887032	-0.6
5000	500	16000	104.157	105.022	21.23315	-23.86236	-1.9
5000	500	16230	55.932	83.858	28.73158	-33.90059	-2.1
5000	500	16500	32.601	60.012	44.51169	-46.87582	-1.9
5000	500	17300	13.781	18.308	145.6153	31.88757	0.7
5000	500	18000	11.111	-7.812	34.85609	63.861725	5.2
5000	500	18200	11.524	-15.693	24.15344	52.097101	6.2
5000	500	18340	12.24	-21.854	19.4067	44.469539	6.4
5000	500	18500	13.664	-29.72	15.80644	36.586413	6.1
5000	500	19300	61.154	-98.154	11.66204	5.8024262	1.2
5000	500	19800	226.938	15.465	15.7209	-11.53092	-1
5000	500	20100	107.867	101.818	21.44881	-23.1536	-1.6
5000	500	20300	62.826	86.177	27.62964	-31.59121	-1.8
5000	500	20700	29.144	53.312	52.67647	-49.7558	-1.6
5000	500	21000	19.994	36.154	94.43312	-52.9411	-0.8
5000	1000	50	42.956	44.24	54.40503	-30.61072	-0.7
5000	1000	200	36.154	38.298	65.42857	-30.47976	-0.5
5000	1000	900	21.594	12.977	95.12118	29.729796	1.7
5000	1000	1500	19.912	-6.694	45.86287	47.876235	4.1
5000	1000	1775	21.698	-16.554	32.32606	39.640251	4.8
5000	1000	1900	23.224	-21.368	28.28669	35.397066	4.7
5000	1000	2300	33.505	-38.844	20.98165	21.930481	3.6
5000	1000	2700	61.556	-56.767	19.03973	9.4512432	1.9
5000	1000	3500	85.217	54.808	32.2362	-20.33109	-0.7
5000	1000	4000	53.441	50.62	44.51002	-28.19423	-1
5000	1000	4125	44.996	45.963	51.7943	-30.40648	-0.8
5000	1000	5000	21.425	13.331	96.47789	29.197911	1.5
5000	1000	5700	19.955	-10.233	39.77598	45.814561	4.4
5000	1000	5920	21.689	-18.272	30.44958	38.646872	4.7
5000	1000	6500	37.374	-44.048	19.76872	18.945727	3.2
5000	1000	7000	88.105	-59.689	19.13407	3.5653998	1.1
5000	1000	7500	130.912	25.199	24.37523	-11.49616	-0.4
5000	1000	7960	66.312	56.412	37.26632	-25.30527	-0.9
5000	1000	8300	40.554	44.108	56.28741	-32.30443	-0.8
5000	1000	9000	21.993	17.156	103.0078	16.231204	1.2
5000	1000	9800	19.391	-9.918	39.92929	46.922295	4.5
5000	1000	9980	20.65	-16.617	31.62264	40.813696	4.8
5000	1000	10500	31.819	-39.421	20.21821	22.546145	3.7
5000	1000	11000	72.131	-62.058	18.39346	6.707948	1.5
5000	1000	11800	103.272	53.107	28.35554	-17.55773	-0.8
5000	1000	12200	53.375	52.548	43.57256	-29.07305	-1

5000	1000	12400	40.465	44.331	56.16423	-32.5437	-0.9
5000	1000	13000	23.254	20.781	103.044	2.0259581	0.7
5000	1000	13800	18.989	-6.391	45.98033	49.833361	4.2
5000	1000	14226	22.371	-22.294	27.00684	35.668884	4.9
5000	1000	14300	23.557	-25.332	25.17729	33.056869	4.7
5000	1000	14700	36.198	-44.202	19.42552	19.381714	3.2
5000	1000	15000	59.384	-58.669	18.38641	9.8724801	1.8
5000	1000	15950	95.1	55.432	29.79388	-18.96642	-0.9
5000	1000	16140	69.059	56.912	36.2456	-24.59061	-1
5000	1000	16500	40.852	44.108	56.02703	-32.0591	-0.8
5000	1000	17000	25.218	24.317	97.42372	-10.31979	0.2
5000	1000	18000	19.684	-9.677	40.52622	46.613764	4.3
5000	1000	18320	22.595	-21.486	27.85422	35.934324	4.8
5000	1000	18400	23.942	-24.912	25.7016	32.985562	4.5
5000	1000	18650	30.175	-35.937	21.35953	24.485586	3.9
5000	1000	19000	49.428	-53.081	18.83463	13.212785	2.4
5000	1000	20100	88.924	55.361	31.20656	-19.82629	-0.9
5000	1000	20350	58.618	53.214	41.1085	-26.9597	-1
5000	1000	20500	47.667	48.15	48.74887	-30.02567	-0.9
5000	1000	21000	27.821	28.382	88.31418	-20.52754	0
5000	1500	50	48.335	29.781	56.20324	-15.27864	0.1
5000	1500	250	41.285	25.83	64.70725	-11.76377	0.4
5000	1500	900	29.598	9.352	72.56783	20.941158	1.8
5000	1500	1200	28.178	1.378	60.58683	31.519708	2.6
5000	1500	1400	28.381	-3.993	51.55891	33.333702	3.1
5000	1500	1880	33.108	-17.368	35.30159	27.451268	3.6
5000	1500	2200	41.168	-26.127	29.54007	20.291363	3
5000	1500	2700	66.474	-32.115	26.6334	8.3654876	1.7
5000	1500	3500	85.847	20.503	34.5537	-9.421499	0.1
5000	1500	4000	55.753	32.055	49.56903	-15.91103	-0.1
5000	1500	5000	29.397	9.701	73.40002	20.732015	1.8
5000	1500	5500	28.052	-3.94	51.71621	33.844254	3.1
5000	1500	6000	33.11	-18.217	34.52554	27.331806	3.6
5000	1500	6500	48.921	-31.067	27.3332	15.655107	2.6
5000	1500	7400	94.021	4.896	30.72316	-5.515779	0.3
5000	1500	8150	53.153	32.456	51.46612	-16.68825	-0.1
5000	1500	8400	42.806	27.993	62.48846	-14.31973	0.2
5000	1500	9000	29.991	12.643	76.61909	15.123962	1.5
5000	1500	9700	28.048	-6.622	47.60438	34.163865	3.3
5000	1500	10000	30.906	-15.351	36.96465	29.923923	3.7
5000	1500	10100	32.554	-18.293	34.36966	27.830643	3.6
5000	1500	10400	40.014	-26.719	29.04545	20.963261	3.1
5000	1500	10600	48.288	-31.61	27.03472	15.943689	2.6

5000	1500	11000	73.406	-32.091	26.16017	6.1347196	1.5
5000	1500	11600	92.181	13.56	32.10601	-7.659384	0.2
5000	1500	12000	67.872	32.991	42.00902	-14.91025	-0.1
5000	1500	13000	31.202	15.447	77.57716	8.6511222	1.2
5000	1500	13850	28.248	-7.958	45.67795	33.893673	3.5
5000	1500	14100	30.834	-15.321	36.98814	30.008562	3.7
5000	1500	14700	48.089	-31.589	27.034	16.047364	2.7
5000	1500	15000	66.078	-33.996	26.00453	8.6149194	1.9
5000	1500	15300	87.111	-22.401	27.14948	1.3741634	1
5000	1500	15700	92.274	13.481	32.06963	-7.639011	0.2
5000	1500	16000	74.778	30.867	38.88782	-13.3864	-0.1
5000	1500	16800	37.174	23.387	70.67848	-8.259884	0.5
5000	1500	17000	32.983	18.184	76.35449	2.1224765	1
5000	1500	17400	28.421	7.471	71.11792	25.379977	2.1
5000	1500	17700	27.547	-0.778561	57.16554	33.737254	2.9
5000	1500	18000	28.723	-9.233	43.94953	33.202225	3.6
5000	1500	18300	32.471	-17.822	34.7969	27.9963	3.7
5000	1500	18500	36.915	-23.745	30.63924	23.453013	3.4
5000	1500	19000	58.564	-33.745	26.30518	11.3796	2.1
5000	1500	19300	79.252	-28.515	26.62849	4.1333025	1.3
5000	1500	19700	94.449	2.916	30.35964	-5.058559	0.5
5000	1500	20150	72.204	31.281	40.01788	-13.71318	-0.1
5000	1500	20800	40.381	25.992	65.86381	-12.07077	0.4
5000	1500	21000	35.34	21.028	73.32933	-4.025553	0.8
5000	2000	50	51.001	16.309	52.88399	-2.832372	0.7
5000	2000	500	42.357	12.077	59.3319	4.8701673	1.2
5000	2000	1000	37.794	4.131	57.09955	16.252913	1.9
5000	2000	1400	37.831	-2.944	49.56547	20.656054	2.4
5000	2000	1650	39.498	-7.277	44.58861	20.560759	2.6
5000	2000	2100	46.11	-13.716	37.81565	16.574516	2.4
5000	2000	2500	55.789	-15.406	34.98118	11.014081	2
5000	2000	3000	67.742	-6.832	35.64857	3.5939189	1.3
5000	2000	3500	67.189	9.119	40.70531	-2.448133	0.8
5000	2000	3925	57.062	16.23	48.17637	-4.234441	0.7
5000	2000	3400	45.856	14.766	57.10331	0.3377598	0.8
5000	2000	4600	42.47	12.354	59.37696	4.5084086	1.2
5000	2000	5000	38.231	6.012	58.62202	14.186664	1.8
5000	2000	5690	38.745	-6.374	45.69683	21.023819	2.6
5000	2000	6250	46.896	-14.403	37.20664	16.148089	2.4
5000	2000	7000	66.125	-9.901	34.98707	5.0658404	1.4
5000	2000	7450	69.515	4.633	38.56601	-1.047596	0.9
5000	2000	7850	61.911	14.709	44.73368	-4.250704	0.6
5000	2000	8400	47.856	15.998	55.61199	-1.602047	0.8

5000	2000	8900	39.707	9.566	60.34864	9.3740348	1.5
5000	2000	9400	36.996	0.826972	54.12504	19.518454	2.2
5000	2000	10050	41.305	-10.764	41.00219	19.772322	2.6
5000	2000	10500	50.233	-15.831	35.7398	14.22995	2.1
5000	2000	11000	64.002	-12.569	34.47787	6.5901052	1.6
5000	2000	11500	70.079	2.721	37.833	-0.43377	0.9
5000	2000	11910	63.138	14.111	43.89771	-4.146163	0.6
5000	2000	12500	47.795	16.107	55.70235	-1.685949	0.9
5000	2000	13000	39.674	9.692	60.4836	9.2660446	1.5
5000	2000	13250	37.608	5.381	58.55179	15.375624	1.9
5000	2000	14000	39.301	-8.302	43.67175	21.03175	2.6
5000	2000	14500	47.737	-15.266	36.49399	15.727242	2.3
5000	2000	15000	61.377	-14.494	34.26078	8.153539	1.6
5000	2000	15800	67.989	9.321	40.36837	-2.717024	0.7
5000	2000	16080	61.391	15.443	45.18281	-4.585554	0.6
5000	2000	16400	52.736	17.186	51.64135	-3.998275	0.7
5000	2000	16900	42.327	12.809	59.78998	4.1017705	1.1
5000	2000	17200	38.749	8.125	60.10849	11.666015	1.6
5000	2000	17900	37.662	-4.576	47.91699	21.515831	2.5
5000	2000	18300	41.786	-11.396	40.37832	19.492412	2.6
5000	2000	18500	45.332	-14.097	37.67622	17.206044	2.5
5000	2000	19000	58.068	-15.722	34.37637	9.9466117	1.8
5000	2000	19800	69.582	5.677	38.79631	-1.485531	0.9
5000	2000	20100	63.821	13.748	43.43421	-4.073432	0.6
5000	2000	20700	48.271	16.284	55.30129	-2.00684	0.9
5000	2000	21000	42.621	12.992	59.57624	3.7351223	1.2
5000	2500	50	51.432	7.703	49.24147	3.6878477	1.3
5000	2500	500	47.118	6.267	51.53128	7.0542872	1.6
5000	2500	1000	44.532	2.348	50.62239	11.555131	1.8
5000	2500	1500	44.982	-2.217	46.83557	13.782431	2
5000	2500	1750	46.355	-4.204	44.70421	13.63602	2.1
5000	2500	2400	52.623	-6.296	40.89459	10.313537	1.8
5000	2500	2700	55.789	-4.912	40.49503	8.0567513	1.7
5000	2500	3200	58.527	0.423824	41.9069	4.5199675	1.4
5000	2500	3700	56.208	5.942	45.45254	2.6764016	1.2
5000	2500	4300	49.954	7.682	50.26658	4.4339187	1.4
5000	2500	4600	47.158	6.412	51.58943	6.923505	1.5
5000	2500	5000	44.768	3.354	51.22144	10.711972	1.8
5000	2500	5600	44.863	-2.266	46.85541	13.900796	2.1
5000	2500	6500	52.608	-6.401	40.83803	10.36239	1.9
5000	2500	7000	57.466	-3.198	40.69899	6.5569635	1.6
5000	2500	7500	58.319	2.864	43.04364	3.4501017	1.3
5000	2500	8000	54.346	7.309	47.1436	2.6364678	1.2

5000	2500	8500	48.923	7.482	50.90625	5.1216727	1.4
5000	2500	8800	46.352	5.856	51.83301	7.8399999	1.6
5000	2500	9500	44.221	-0.321972	48.72566	13.401535	2
5000	2500	9750	44.968	-2.651	46.50439	14.003925	2.1
5000	2500	10600	52.548	-6.554	40.76905	10.454389	1.9
5000	2500	11500	58.682	1.546	42.31393	3.938386	1.3
5000	2500	12175	53.599	7.626	47.75451	2.7563075	1.2
5000	2500	13000	45.638	5.194	51.91609	8.7984715	1.6
5000	2500	13600	44.154	-0.356331	48.73556	13.474626	2
5000	2500	13870	44.973	-2.864	46.33588	14.100657	2.1
5000	2500	14700	52.517	-6.663	40.71552	10.512783	1.9
5000	2500	15000	55.869	-5.265	40.28018	8.1541649	1.7
5000	2500	15400	58.667	-1.03	41.20118	5.1075191	1.5
5000	2500	16000	56.519	6.073	45.32206	2.4789229	1.2
5000	2500	17000	49.326	6.006	49.80634	5.947795	1.6
5000	2500	17500	44.102	1.688	50.38609	12.309656	1.9
5000	2500	17700	44.019	-0.323977	48.83664	13.565681	2.1
5000	2500	19000	54.718	-6.009	40.3041	9.0380251	1.8
5000	2500	20000	57.448	5.01	44.37156	2.6975816	1.3
5000	2500	21000	47.257	6.734	51.70672	6.6256278	1.5

APPENDIX 9. PARASITIC MODELS FOR 0402 INDUCTORS AND CAPACITORS

Inductor parasitic model for 0402 parts

Port
P1
Num=1

C
C6
C=0.0175 pF

L
L2
L=L
R=

C
C4
C=0.039 pF

R
R2
R=4000 Ohm

C
C5
C=0.0175 pF

Port
P2
Num=2
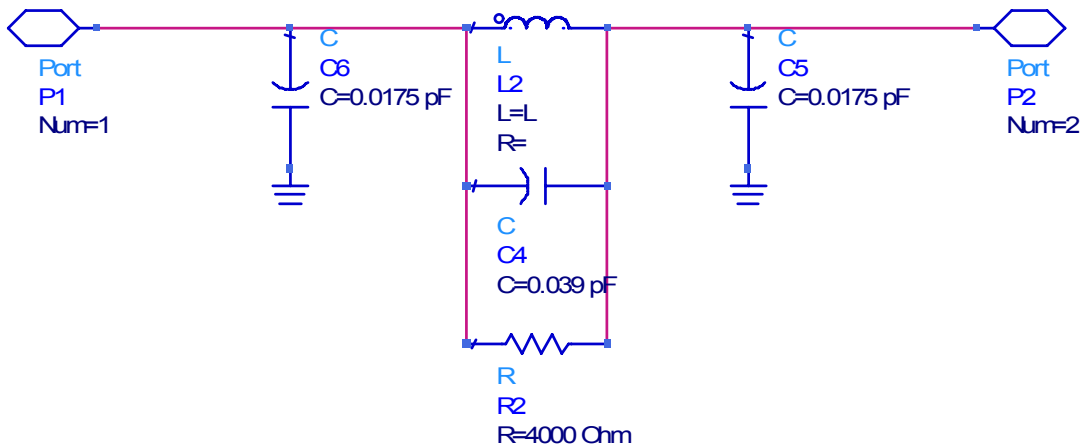
Capacitor parasitic model for 0402 parts

Port
P1
Num=1

C
C2
C=0.0175 pF

C
C1
C=Cap

L
L1
L=0.32 nH
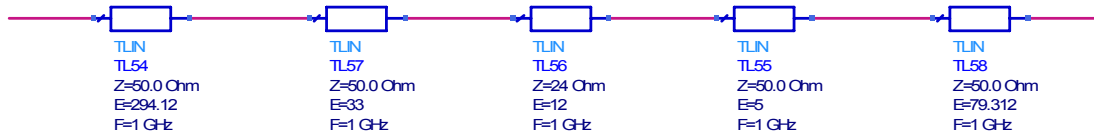R=

C
C3
C=0.0175 pF

Port
P2
Num=2

58
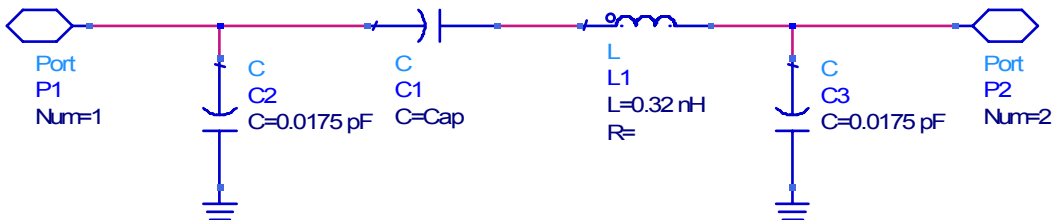
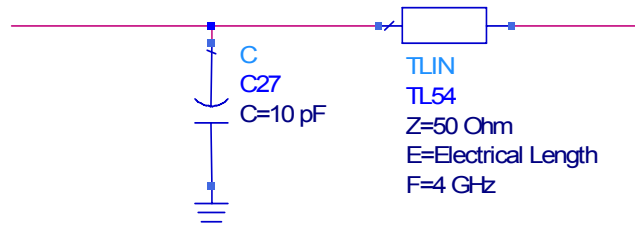## APPENDIX 10: INPUT AND OUTPUT MATCHING CIRCUIT SCHEMATIC
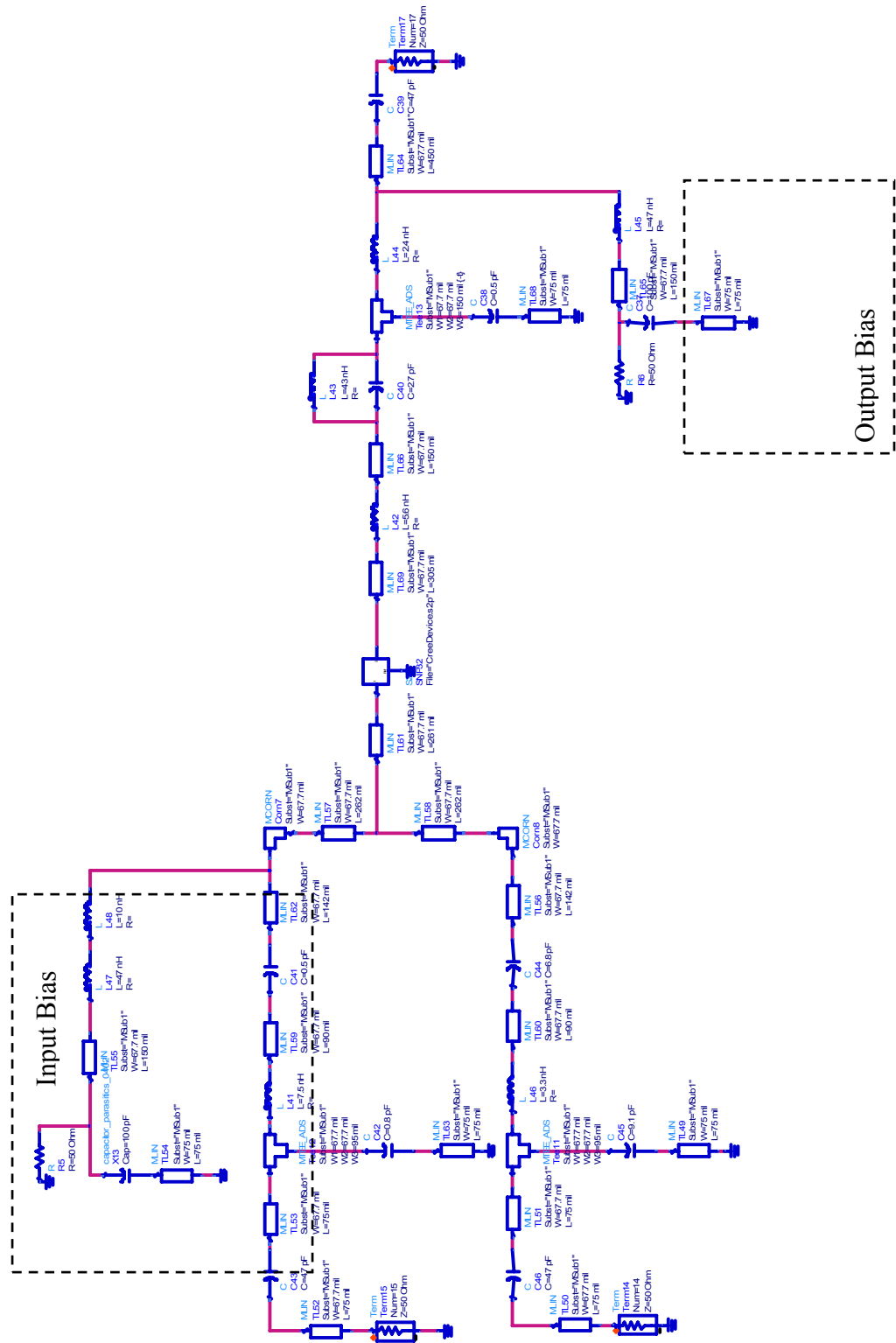
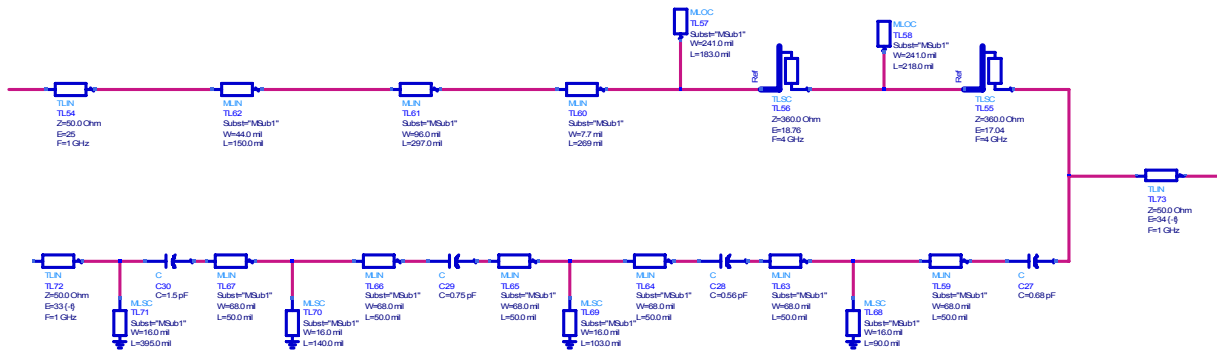# APPENDIX 11: TRANSMISSION LINE APPROXIMATION FOR EACH IMPEDANCE BLOCK USED IN THE SECOND HARMONIC SOURCE PULL SETUP
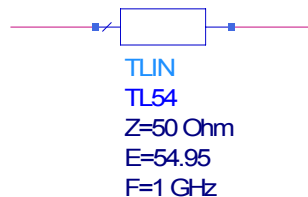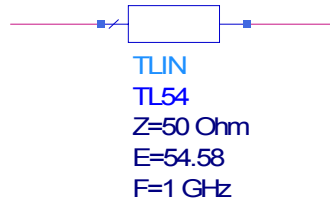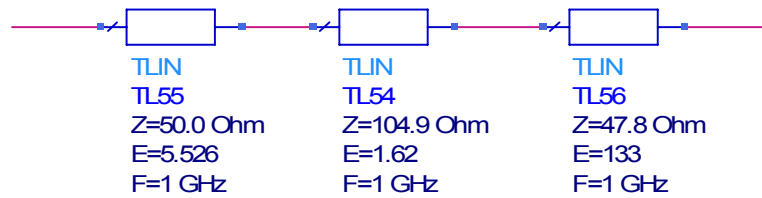
Fundamental Tuner

2nd Harmonic Tuner

Diplexer

Male to Male connector

Input Coupler

TLIN
TL54
Z=50 Ohm
E=54.58
F=1 GHz

Input Half of Test Fixture

TLIN
TL55
Z=50.0 Ohm
E=5.526
F=1 GHz

TLIN
TL54
Z=104.9 Ohm
E=1.62
F=1 GHz

TLIN
TL56
Z=47.8 Ohm
E=133
F=1 GHz

Output Half of Test Fixture

TLIN
TL54
Z=47.8 Ohm
E=133
F=1 GHz

TLIN
TL55
Z=104.9 Ohm
E=1.62
F=1 GHz

TLIN
TL56
Z=50.0 Ohm
E=5.526
F=1 GHz

Output Coupler

TLIN
TL54
Z=50 Ohm
E=108.2
F=1 GHz

Load Tuner

TLIN
TL59
Z=50.0 Ohm
E=72
F=1 GHz

TLIN
TL60
Z=Z1 Ohm
E=3.7
F=1 GHz

TLIN
TL57
Z=48 Ohm
E=90
F=1 GHz

TLIN
TL56
Z=78 Ohm
E=19
F=1 GHz

TLIN
TL55
Z=48 Ohm
E=141
F=1 GHz

TLIN
TL54
Z=Z1 Ohm
E=4.1
F=1 GHz

TLIN
TL58
Z=50.0 Ohm
E=32.5
F=1 GHz
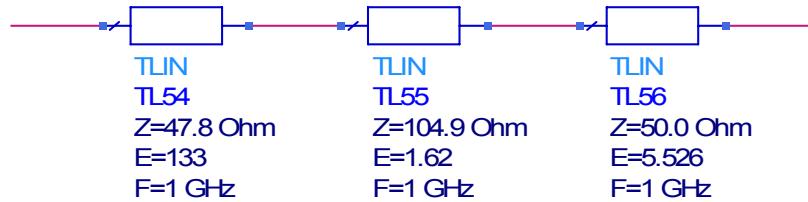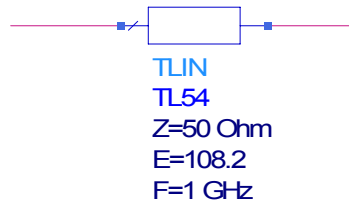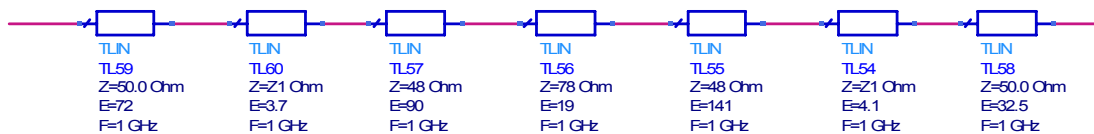
APPENDIX 12: SIMULATED SECOND HARMONIC INPUT IMPEDANCES AND OUTPUT POWER CORRESPONDING TO ELECTRICAL LENGTH OF THE TRANSMISSION LINE USED TO MODEL THE TUNER

Electrical Length	Impedance at Tuner		Impedance at DUT		2nd harmonic power
	Real	Imaginary	Real	Imaginary	
10	0.316	4.795	0.462	35.12	4.466803178
50	0.636	50.838	4.354	172.949	4.89543523
100	34.159	-159.096	0.879	-59.138	5.817957749
120	1.689	-104.906	0.457	-27.131	5.67886296
140	0.615	-49.168	0.342	-8.009	-5.03623946
160	0.378	-22.808	0.325	7.778	2.939915144
180	0.315	-3.954	0.385	24.667	4.025757082
200	0.337	13.845	0.606	48.572	4.482059154
220	0.472	35.634	1.634	100.27	5.279818654
240	0.973	72.683	41.106	540.621	5.126271262
260	4.97	192.916	4.042	-158.826	4.745846751
280	34.159	-519.096	0.879	-59.138	5.525558738
300	1.689	-104.906	0.457	-27.131	5.31992741
320	0.615	-49.168	0.342	-8.009	-5.090696627
340	0.378	-22.808	0.325	7.778	3.610545658
360	0.315	-3.953	0.385	24.668	4.366507932
380	0.337	13.845	0.606	48.572	4.616128569
400	0.472	35.634	1.634	100.27	4.80499263
420	0.973	72.683	41.106	540.621	4.982009544
440	4.97	192.916	4.042	-158.826	5.219353724
460	34.159	-519.096	0.879	-59.138	5.818402284
480	1.689	-104.906	0.457	-27.131	5.676875156
500	0.615	-49.168	0.342	-8.009	-5.03623946
520	0.378	-22.808	0.325	7.778	2.939915144
540	0.315	-3.954	0.385	24.668	4.025757082
560	0.337	13.845	0.606	48.572	4.479259044
580	0.472	35.634	1.634	100.27	5.280575355
600	0.973	72.683	41.106	540.621	5.187098546
620	4.97	192.916	4.042	-158.826	4.740815828
640	34.159	-519.096	0.879	-59.138	5.524823082
660	1.689	-104.906	0.457	-27.131	5.320868919
680	0.615	-49.168	0.342	-8.009	-5.101629151
700	0.378	-22.808	0.325	7.778	3.610774925
720	0.315	-3.954	0.385	24.668	4.366613011

740	0.337	13.845	0.606	48.572	4.614086272
760	0.472	35.634	1.634	100.27	4.805292345
780	0.973	72.683	41.106	540.621	4.984652205
800	4.97	192.916	4.042	-158.826	5.219544227
820	34.159	-519.096	0.879	-59.138	5.818135566
840	1.689	-104.906	0.457	-27.131	5.675971458
860	0.615	-49.168	0.342	-8.009	-5.023839901
880	0.378	-22.808	0.325	7.778	2.939915144
900	0.315	-3.954	0.385	24.668	4.025757082
920	0.337	13.845	0.606	48.572	4.480296227
940	0.472	35.634	1.634	100.27	5.2802916
960	0.973	72.683	41.106	540.621	5.130506497
980	4.97	192.916	4.042	-158.826	4.733767635
1000	34.159	-519.096	0.879	-59.138	5.521511859

APPENDIX 13: PICTURE OF THE BOARD WITH THE MATCHING INPUT AND OUTPUT IMPEDANCES ON THE DEVICE
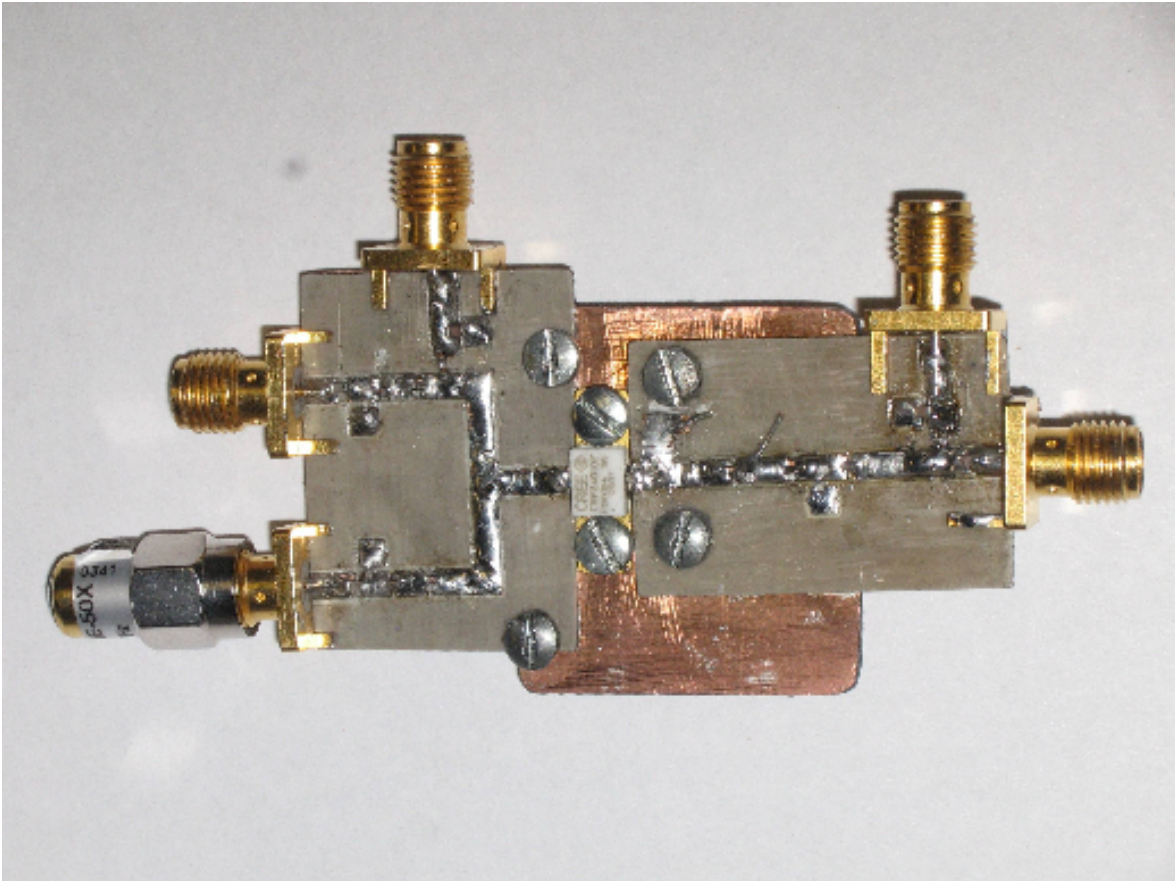
BIBLIOGRAPHY

[1] Maury Microwave Corporation, "Theory of Load and Source Pull Measurement," [Online application notes], (1999 Jul 27), Available at HTTP: http://maurymw.com/support/pdfs/5C-041.pdf

[2] D. C. Yang and D. F. Peterson, "Large-Signal Characterization of Two-Port Nonlinear Active Networks," <u>Transactions on Microwave Theory and Techniques</u>, vol. 30, no. 12, Dec. 1982, pp. 345-347.

[3] J. Sevic, "Introduction to Tuner-Based Measurement and Characterization," [Online technical data], (2004 Aug 31), Available at HTTP: http://www.maurymw.com/support/pdfs/5C-054.pdf

[4] CREE, "CRF24010," [Online datasheet], (2007 Aug), Available at HTTP: http://www.cree.com/products/pdf/CRF24010-Rev1_8.pdf

[5] Maury Microwave Corporation, "Device Characterization with Harmonic Source and Load Pull," [Online application notes], (2000 Dec 7), Available at HTTP: http://www.maurymw.com/support/pdfs/5C-044.pdf

[6] G. R. Simpson and M. Vasser, "Importance of 2nd Harmonic Tuning for Power Amplifier Design," <u>48th ARFTG Conference Digest</u>, vol. 30, Dec. 1996, pp. 1-6.

[7] "Automated Tuner System -MT980 Series: Operating and Service Manual," Ontario, CA: Maury Microwave Corporation, 1995.

[8] S. V. Sekar, H. Cao, and R. J. Weber, "Changes in dc Current Bias as a Function of Input Drive for a Depletion Mode SiC MESFET," presented at IEEE International Conference on Electro/Information Technology. Ames, IA, 2008.

[9] W. R. Curtice, "A MESFET Model for Use in the Design of GaAs Integrated Circuits," <u>IEEE Transactions on Microwave Theory and Techniques</u>, vol. 28, May 1980, pp. 448-456.

[10] R. Ludwig, and P. Bretchko, RF Circuit Theory and Applications, Pearson Education, Inc., 2000, pp. 331-340

[11] R. J. Weber, "Introduction to Microwave Circuits," Piscataway: IEEE Press, 2001

[12] P. Berini, M. Desgagne, F. M. Ghannouchi, and R. G. Basisio, "An Experimental Study of the Effects of Harmonic Loading on Microwave MESFETS Oscillators and Amplifiers," <u>Transactions on Microwave Theory and Techniques</u>, vol. 42, no. 6, Jun. 1994, pp. 943-950.

[13] R. K. Varanasi, C. P. Baylis II, L. P. Dunleavy and Harris Corporation, "Prediction of Harmonic Tuning Performance in p-HEMTs," The 2005 IEEE Annual Conference on Wireless and Microwave Technology, 2005 pp. 183-186.

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